| Exhibit R-2, RDT&E Budget Item Justification: PB 2020 Defense Advanced Research Projects Agency | Date: March 2019 |
|---|---|
| **Appropriation/Budget Activity**<br>0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research* | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* |

| COST ($ in Millions) | Prior Years | FY 2018 | FY 2019 | FY 2020 Base | FY 2020 OCO | FY 2020 Total | FY 2021 | FY 2022 | FY 2023 | FY 2024 | Cost To Complete | Total Cost |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Total Program Element | - | 283.180 | 348.847 | 332.192 | - | 332.192 | 340.000 | 369.456 | 386.366 | 392.366 | - | - |
| ELT-01: *ELECTRONIC TECHNOLOGY* | - | 283.180 | 115.208 | 135.882 | - | 135.882 | 147.300 | 165.556 | 182.156 | 188.156 | - | - |
| ELT-02: *BEYOND SCALING TECHNOLOGY* | - | 0.000 | 233.639 | 196.310 | - | 196.310 | 192.700 | 203.900 | 204.210 | 204.210 | - | - |

**A. Mission Description and Budget Item Justification**

The Electronics Technology Program Element is budgeted in the Applied Research Budget Activity because its objective is to develop electronics that make a wide range of military applications possible. The Electronics Technology Project focuses on turning basic advancements into the underpinning technologies required to address critical national security issues and to enable an information-driven warfighter.

Advances in microelectronic device technologies continue to significantly benefit improved weapons effectiveness, intelligence capabilities, and information superiority. The Electronic Technology project therefore supports continued advancement in microelectronics, including electronic and optoelectronic devices, Microelectromechanical Systems (MEMS), semiconductor device design and fabrication, and new materials and material structures. Particular focuses of this work include reducing the barriers to designing and fabricating custom electronics and exploiting improved manufacturing techniques to provide low-cost, high-performance sensors. Programs in this project will also greatly improve the size, weight, power, and performance characteristics of electronic systems; support positioning, navigation, and timing in GPS-denied environments; and develop sensors more sensitive and robust than today's standards.

The Electronic Technology project will also investigate the feasibility, design, and development of powerful devices, including non-silicon-based materials technologies to achieve low-cost, reliable, fast, and secure computing, communication, and storage systems. Rapid design and utilization of these new technologies will be a critical focus of ELT-01, as DoD looks for mechanisms to speed the development and fielding of advanced technologies.

This project has six major focus areas: Electronics, Photonics, MicroElectroMechanical Systems, Architectures, Algorithms, and other Electronic Technology research.

The Beyond Scaling Technology project recognizes that, within the next decade, the continuous pace of improvements in electronics performance will face the fundamental limits of silicon technology. These limits present a barrier that must be overcome in order for progress to continue. This project will therefore pursue potential electronics performance advancements that do not rely on Moore's Law but instead leverage circuit specialization, to include materials, architectures, and designs intended to suit a specific need. In addition, the Beyond Scaling Technology Project recognizes that the envisioned electronics specialization will require proper security safeguards. Electronics advancements must simultaneously make progress in performance and secure the foundation on which our digital infrastructure relies. Programs within the Beyond Scaling project will look at reducing barriers to making specialized circuits in today's silicon hardware and significantly increase the ease with which DoD can design, deliver, and eventually upgrade critical, customized electronics. Programs will also explore alternatives to traditional circuit architectures,

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for instance by exploiting vertical circuit integration to optimize electronic devices and by incorporating novel materials, and explore techniques for securing DoD and commercial data and hardware.

| B. Program Change Summary ($ in Millions) | FY 2018 | FY 2019 | FY 2020 Base | FY 2020 OCO | FY 2020 Total |
|---|---|---|---|---|---|
| Previous President's Budget | 295.447 | 333.847 | 307.073 | - | 307.073 |
| Current President's Budget | 283.180 | 348.847 | 332.192 | - | 332.192 |
| Total Adjustments | -12.267 | 15.000 | 25.119 | - | 25.119 |
| • Congressional General Reductions | 0.000 | -15.000 | | | |
| • Congressional Directed Reductions | 0.000 | 0.000 | | | |
| • Congressional Rescissions | 0.000 | 0.000 | | | |
| • Congressional Adds | 0.000 | 30.000 | | | |
| • Congressional Directed Transfers | 0.000 | 0.000 | | | |
| • Reprogrammings | 0.000 | 0.000 | | | |
| • SBIR/STTR Transfer | -12.267 | 0.000 | | | |
| • TotalOtherAdjustments | - | - | 25.119 | - | 25.119 |

| Congressional Add Details ($ in Millions, and Includes General Reductions) | FY 2018 | FY 2019 |
|---|---|---|
| **Project:** ELT-02: *BEYOND SCALING TECHNOLOGY* | | |
| Congressional Add: *DARPA Electronics Resurgence Initiative* | - | 30.000 |
| Congressional Add Subtotals for Project: ELT-02 | - | 30.000 |
| Congressional Add Totals for all Projects | - | 30.000 |

**Change Summary Explanation**

FY 2018: Decrease reflects SBIR/STTR transfer.

FY 2019: Increase reflects Congressional adjustments.

FY 2020: Increase reflects initiation of the Intelligent Spectroscopic & Temporal Fusion (INSPECT) and Instinctual RF programs in FY 2020.

| Exhibit R-2A, RDT&E Project Justification: PB 2020 Defense Advanced Research Projects Agency | | | Date: March 2019 |
|---|---|---|---|
| Appropriation/Budget Activity<br>0400 / 2 | R-1 Program Element (Number/Name)<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | Project (Number/Name)<br>ELT-01 / *ELECTRONIC TECHNOLOGY* | |

| COST ($ in Millions) | Prior Years | FY 2018 | FY 2019 | FY 2020 Base | FY 2020 OCO | FY 2020 Total | FY 2021 | FY 2022 | FY 2023 | FY 2024 | Cost To Complete | Total Cost |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ELT-01: *ELECTRONIC TECHNOLOGY* | - | 283.180 | 115.208 | 135.882 | - | 135.882 | 147.300 | 165.556 | 182.156 | 188.156 | - | - |

**A. Mission Description and Budget Item Justification**

Advances in microelectronic device technologies continue to significantly benefit improved weapons effectiveness, intelligence capabilities, and information superiority. The Electronic Technology project therefore supports continued advancement in microelectronics, including electronic and optoelectronic devices, Microelectromechanical Systems (MEMS), semiconductor device design and fabrication, and new materials and material structures. Particular focuses of this work include reducing the barriers to designing and fabricating custom electronics and exploiting improved manufacturing techniques to provide low-cost, high-performance sensors. Programs in this project will also greatly improve the size, weight, power, and performance characteristics of electronic systems; support positioning, navigation, and timing in GPS-denied environments; and develop sensors more sensitive and robust than today's standards.

The Electronic Technology project will also investigate the feasibility, design, and development of powerful devices, including non-silicon-based materials technologies to achieve low-cost, reliable, fast, and secure computing, communication, and storage systems. Rapid design and utilization of these new technologies will be a critical focus of ELT-01, as DoD looks for mechanisms to speed the development and fielding of advanced technologies.

This project has six major focus areas: Electronics, Photonics, MicroElectroMechanical Systems, Architectures, Algorithms, and other Electronic Technology research.

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| ***Title:*** High power Amplifier using Vacuum electronics for Overmatch Capability (HAVOC) | 18.000 | 6.000 | 5.000 |
| ***Description:*** The High power Amplifier using Vacuum electronics for Overmatch Capability (HAVOC) program seeks to develop compact Radio Frequency (RF) signal amplifiers for air, ground, and ship-based communications and sensing systems. HAVOC amplifiers would enable these systems to access the high-frequency millimeter-wave portion of the Electromagnetic (EM) spectrum, facilitating increased range and other performance improvements. Today, the effectiveness of combat operations across all domains increasingly depends on DoD's ability to control and exploit the EM spectrum and to deny its use to adversaries. However, the proliferation of inexpensive commercial RF sources has made the EM spectrum crowded and contested, challenging our spectrum dominance. Operating at higher frequencies, such as the millimeter-wave, helps DoD to overcome these issues and offers numerous tactical advantages such as high data-rate communications and high resolution and sensitivity for radar and sensors. Opportunities for transferring HAVOC technology to the Services will be identified during the execution of the early phases of the program. Technology transfer efforts will follow a spiral development process to mitigate risk and provide the opportunity to incorporate new technological developments as they occur. Basic research for this program is funded within PE 0601101E, Project ES-01. | | | |
| ***FY 2019 Plans:*** | | | |

| Exhibit R-2A, RDT&E Project Justification: PB 2020 Defense Advanced Research Projects Agency | | Date: March 2019 |
|---|---|---|
| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-01 / *ELECTRONIC TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| - Complete the design, fabrication, and testing of higher power, higher duty cycle devices to meet Phase 2 program metrics.<br>- Research novel techniques and technologies to address greater thermal management requirements of higher power devices.<br>- Fabricate and test higher power, higher duty cycle devices to meet Phase 3 program metrics.<br>***FY 2020 Plans:***<br>- Transition designs and prototypes to the Services.<br>***FY 2019 to FY 2020 Increase/Decrease Statement:***<br>The FY 2020 decrease reflects the program transitioning from fabrication and testing of devices to transition. | | | |
| ***Title:*** Precise Robust Inertial Guidance for Munitions (PRIGM) | 18.500 | 10.500 | 8.000 |
| ***Description:*** The Precise Robust Inertial Guidance for Munitions (PRIGM) program aims to develop inertial sensor technologies for positioning, navigation, and timing (PNT) in GPS-denied environments. When GPS is not available, these inertial sensors can provide autonomous PNT information. The program will exploit recent advances in integrating photonic (light-manipulating) components into electronics and in employing Microelectromechanical Systems (MEMS) as high-performance inertial sensors for use in extreme environments. Whereas conventional MEMS inertial sensors can suffer from inaccuracies due to factors such as temperature sensitivity, new photonics-based PNT techniques have demonstrated the ability to mitigate these inaccuracies. PRIGM will focus on two areas. By 2020, it aims to develop and transition a Navigation-Grade Inertial Measurement Unit (NGIMU), a state-of-the-art MEMS device, to DoD platforms. By 2030, it aims to develop Advanced Inertial MEMS Sensors (AIMS) that can provide gun-hard, high-bandwidth, high dynamic range navigation for GPS-free munitions. These advances should enable navigation applications, such as smart munitions, that require low-cost, size, weight, and power inertial sensors with high bandwidth, precision, and shock tolerance. PRIGM will advance state-of-the-art MEMS gyros from TRL-3 devices to a TRL-6 transition platform, eventually enabling the Service Labs to perform TRL-7 field demonstrations. Basic research for this program is funded within PE 0601101E, Project ES-01 and advanced technology development for the program is budgeted in PE 0603739E, Project MT-15.<br>***FY 2019 Plans:***<br>- Demonstrate 100x increase in frequency stability and 3x reduction in power consumption in MEMS clock oscillators.<br>- Package all component technology and test photonic-MEMS inertial sensor performance, robustness to environmental temperature variation, and repeatability between routine operations.<br>***FY 2020 Plans:***<br>- Demonstrate inertial sensor survival and operation through laboratory-representative launch events.<br>***FY 2019 to FY 2020 Increase/Decrease Statement:*** | | | |

| Exhibit R-2A, RDT&E Project Justification: PB 2020 Defense Advanced Research Projects Agency | | Date: March 2019 |
|---|---|---|
| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-01 / *ELECTRONIC TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| The decrease in FY 2020 reflects completion of design to transition of packaging component technology and testing inertial sensor performance. | | | |
| ***Title:*** Wafer-scale Infrared Detectors (WIRED)<br><br>***Description:*** The WIRED program addresses the need for low-cost, high-performance imaging sensors in the short-wave and mid-wave infrared (SWIR/MWIR) bands. These sensors will provide increased standoff distances for small unmanned aerial vehicles, low-cost missiles, handheld weapon sights and surveillance systems, helmet-mounted systems, and ground-vehicle-mounted threat warning systems. WIRED proposes to manufacture these sensors at the wafer scale, which reduces costs by processing dozens to hundreds of camera imaging arrays at a time. Wafer-scale manufacturing has already driven a revolution in optical imaging in both the visible and the Long-Wave Infrared (LWIR) spectrum, with high-resolution digital cameras and LWIR sensors having become commonplace or widely-available. However, no similar technologies exist for the SWIR/MWIR bands. WIRED could therefore drive a similar revolution in SWIR/MWIR. The program aims to significantly reduce the weight and volume of MWIR detectors, which today require heavy cryogenic cooling systems, and increase the resolution of SWIR detectors by dramatically reducing their pixel size relative to the state-of-the-art.<br><br>***FY 2019 Plans:***<br>- Demonstrate an integrated MWIR camera and evaluate performance at temperature of 270 K.<br>- Demonstrate an integrated small-pitch SWIR camera and optimize design of high-resolution SWIR camera.<br><br>***FY 2020 Plans:***<br>- Demonstrate improved performance of a both the MWIR and SWIR cameras.<br><br>***FY 2019 to FY 2020 Increase/Decrease Statement:***<br>The FY 2020 decrease reflects the program transitioning to final demonstrations. | 19.000 | 15.000 | 7.682 |
| ***Title:*** Modular Optical Aperture Building Blocks (MOABB)<br><br>***Description:*** The Modular Optical Aperture Building Blocks (MOABB) program aims to greatly improve the cost, size, weight, and performance of free-space optical systems. These systems enable applications such as Light Detection And Ranging (LIDAR), laser communications, laser illumination, navigation, and 3D imaging. Specifically, MOABB will construct millimeter-scale optical building blocks that can be coherently arrayed to form larger, higher power devices. These building blocks would replace the traditional large and expensive precision lenses and mirrors, which require slow mechanical steering, that form conventional optical systems. MOABB will develop scalable optical phased arrays that can steer light waves without the use of mechanical components. These advances would allow for a 100-fold reduction in size and weight and a 1,000-fold increase in the steering rate of optical systems.<br><br>***FY 2019 Plans:*** | 21.000 | 20.000 | 20.000 |

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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-01 / *ELECTRONIC TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| - Demonstrate frequency modulated LIDAR functionality of a unit cell.<br>- Improve the aperture size, output power, field of regard, and efficiency of optical phased array transmitters.<br>- Co-package optical phased arrays with chip-scale laser sources.<br>***FY 2020 Plans:***<br>- Synthesize multiple light beams from a single optical phased array aperture of one square centimeter area.<br>- Demonstrate integration of laser sources and optical phased arrays on a single photonic chip.<br>- Characterize and deliver a prototype LIDAR module using optical phased arrays. | | | |
| ***Title:*** Atomic Clock with Enhanced Stability (ACES)<br>***Description:*** The Atomic Clock with Enhanced Stability (ACES) program aims to develop extremely stable chip-scale atomic clocks for unmanned aerial vehicles and other low size, weight, and power (SWaP) platforms with extended mission durations. Atomic clocks provide the high-performance backbone of timing and synchronization for DoD navigation; communications; electronic warfare (EW); and intelligence, surveillance, and reconnaissance (ISR) systems. However, atomic clocks are limited, particularly by temperature sensitivity, aging over long timescales, and a loss of accuracy when power cycled. By employing alternative approaches to confining and measuring atomic particles, ACES could yield a 100x - 1,000x improvement in key performance parameters related to each of these limitations. ACES will also focus on developing the component technologies necessary for low-cost manufacturing and for deployment in harsh DoD-relevant environments. Among its many benefits, program success could help reduce the risk posed by a growing national dependence on GPS, allowing systems to maintain their timing accuracy in the event of temporary GPS unavailability.<br>***FY 2019 Plans:***<br>- Complete fabrication and testing of an integrated physics package meeting the ACES Phase 2 SWaP, retrace, aging, and instability goals.<br>- Deliver prototype physics package and supporting electronics to government facility for testing.<br>***FY 2020 Plans:***<br>- Design an integrated physics package meeting Phase 3 SWaP objectives such that prototypes can be completed and tested.<br>***FY 2019 to FY 2020 Increase/Decrease Statement:***<br>The FY 2020 decrease reflects ACES completing fabrication and conducting final testing for transition to the Service Labs for further development. | 21.000 | 16.000 | 6.000 |
| ***Title:*** Limits of Thermal Sensors (LOTS)<br>***Description:*** The Limits of Thermal Sensors (LOTS) program aims to demonstrate long-wave infrared (LWIR) detector technologies with both high performance and low-size, weight, power, and cost (SWaP-C). The resulting technologies would | 9.000 | 7.668 | 7.000 |

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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-01 / *ELECTRONIC TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| enable improvements in imaging systems such as night-vision goggles, infrared-guided missiles, and missile threat warning systems. Currently, LWIR-enabled systems must choose between large and expensive cryogenically-cooled detectors, which offer high sensitivity and low response times, and uncooled detectors called microbolometers, which offer significant SWaP-C reductions at lower performance. LOTS seeks to develop microbolometers that can compete with larger cameras in terms of higher sensitivity required to detect signals over long ranges and lower response time required to avoid image blur. These technologies will allow DoD to deploy smaller, lighter, and cheaper sensors on critical, high-value assets while maintaining or improving their ability to engage fast-moving or distant targets.<br><br>***FY 2019 Plans:***<br>- Build LWIR cameras with refined sensors to meet final program specifications.<br>- Validate test camera sensitivity and response time in a relevant application environment.<br><br>***FY 2020 Plans:***<br>- Validate improved robustness of the test camera in response to relevant radiation conditions.<br><br>***FY 2019 to FY 2020 Increase/Decrease Statement:***<br>The FY 2020 decrease reflects the program transitioning from refining sensors to validating test camera hardening performance. | | | |
| ***Title:*** Atomic Magnetometry for Biological Imaging In Earth's Native Terrain (AMBIIENT) | 12.000 | 11.540 | 14.000 |
| ***Description:*** The Atomic Magnetometry for Biological Imaging In Earth's Native Terrain (AMBIIENT) program will develop novel magnetic sensors capable of providing high-sensitivity signal measurements in the presence of ambient magnetic fields. In recent years, the value of magnetic imaging, for example for cardiac and other biological signals, has shown tremendous potential for advanced research and clinical diagnosis. Practical application, however, has been limited. Interference from natural and manmade ambient magnetic fields has required that the measurements be performed in specialized, magnetically-shielded research facilities. The AMBIIENT program will exploit novel physical architectures that are resistant to the impact of common noise sources. The AMBIIENT sensor itself must be able to detect the gradient of a local magnetic field while subtracting the much larger ambient signal. This would enable low-cost, portable, high-sensitivity measurements for in-the-field applications. In addition to medical research and clinical diagnosis, AMBIIENT sensors promise to enable diverse sensing applications including magnetic gradient navigation, anomaly detection, perimeter monitoring, and Ultralow Frequency (ULF) communications.<br><br>***FY 2019 Plans:***<br>- Fabricate and test preliminary architectures for direct gradient sensing of magnetic fields.<br>- Refine quantitative models of gradient sensor physics. | | | |

| Exhibit R-2A, RDT&E Project Justification: PB 2020 Defense Advanced Research Projects Agency | | Date: March 2019 |
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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-01 / *ELECTRONIC TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| - Perform laboratory testing of proof-of-principle gradient sensor physics package meeting AMBIIENT Phase 1 size weight and power, accuracy, and sensitivity goals.<br>***FY 2020 Plans:***<br>- Design sensor package architecture meeting AMBIIENT Phase 2 size weight and power, accuracy, and sensitivity goals.<br>- Fabricate and test Phase 2 architectures for direct gradient sensing of magnetic fields.<br>***FY 2019 to FY 2020 Increase/Decrease Statement:***<br>The FY 2020 increase reflects a shift from initial testing to sensor package architecture fabrication. | | | |
| ***Title:*** Dynamic Range-enhanced Electronics and Materials (DREaM)<br>***Description:*** The Dynamic Range-enhanced Electronics and Materials (DREaM) program aims to develop intrinsically linear (ideal) radio frequency (RF) transistors with improved power efficiency and extremely high dynamic range. Linearity, power efficiency, and dynamic range are fundamental characteristics that allow RF systems to reliably transmit clear signals. Improving these characteristics is essential to operating in a crowded RF environment and to enabling next-generation communication, sensing, and electronic warfare systems. Traditional RF transistor designs typically require a trade-off between linearity and broadcast power, and poor linearity results in undesired interference. DREAM will overcome this tradeoff by employing new transistor materials, architectures, and designs. The resulting DREAM-enabled technologies will allow future RF electronics to increase their operating range without polluting the already-congested RF spectrum and while consuming less system power.<br>***FY 2019 Plans:***<br>- Develop initial low noise and lower power consumption linear transistor prototype that provides 10 times improvement of linearity figure of merit than the state of the art.<br>- Demonstrate fabrication processes for initial advanced transistor architectures and complete early characterization of RF transistor prototypes with two times improvement in output power over the state of the art.<br>***FY 2020 Plans:***<br>- Manufacture and characterize transistor unit cells with both a three times improvement over the state of the art in output power density and 10 times higher linearity.<br>- Optimize fabrication processes and explore novel transistor topology to enable higher breakdown voltage, for design of transistors with four times higher power density than the state of the art.<br>- Exploit new channel materials and perform device modeling to enable scaling to 30 times higher linearity than state of the art at 30 gigahertz operational frequency.<br>***FY 2019 to FY 2020 Increase/Decrease Statement:*** | 14.000 | 15.000 | 16.000 |

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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-01 / *ELECTRONIC TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| The FY 2020 increase reflects the program transitioning from developing advanced transistor architectures to manufacturing transistor unit cells. | | | |
| ***Title:*** Wideband Secured and Protected Emitter and Receiver (WiSPER)* | - | 6.000 | 17.000 |
| ***Description:*** *formerly Ensured Communication Link for Identification Friend or Foe (ECLIFF)<br><br>The Wideband Secured and Protected Emitter and Receiver (WiSPER) program aims to develop an ultra-broadband technology platform to demonstrate a robust, secure and protected communication link. WiSPER technology provides high signal coding gain to deliver a secured and protected link with significantly enhanced capacity for next generation DoD communications. Current terrestrial tactical radios operate with limited bandwidth at prescribed low frequency bands, which are unable to support high capacity with multiple users, and vulnerable to interference and jamming. WISPER technology addresses military needs for assured communications, electronic warfare (EW) communications deception, throughput, security, and size, weight, and power (SWaP) limitations of future C4ISR missions. The program develops an ultra-broadband compact antenna, radio frequency front end electronics, mixed signal circuits, and featureless waveform technologies. The WiSPER program will culminate with the integration and demonstration of a secured communication link. The WiSPER program moved from ELT-02, Beyond Scaling Technologies, in FY 2019.<br><br>***FY 2019 Plans:***<br>- Complete system study of secured transceiver architecture for ultra-broadband communication links.<br>- Begin initial designs of antenna, integrated circuits, and waveform to implement ultra-broadband communications.<br><br>***FY 2020 Plans:***<br>- Develop and fabricate components of the 1st-generation of transceivers.<br>- Integrate the 1st-generation prototype transceivers.<br>- Demonstrate prototype secured radio link operation in laboratory testing environment.<br><br>***FY 2019 to FY 2020 Increase/Decrease Statement:***<br>The FY 2020 increase reflects the program shifting from initial designs of antenna, and integrated circuits to developing and fabricating components of the 1st-generation of transceivers. | | | |
| ***Title:*** SHort Range Independent Microrobotic Platforms (SHRIMP) | - | 4.500 | 12.000 |
| ***Description:*** The SHort Range Independent Microrobotic Platforms (SHRIMP) program will develop and demonstrate multi-functional millimeter-to-centimeter scale robotic platforms with a focus on untethered mobility, maneuverability, and dexterity. To achieve this goal, SHRIMP will also provide foundational research in the area of micro-actuator materials and energy efficient power systems for extremely size, weight, and power (SWaP)-constrained microrobotic systems. The program's platform | | | |

| Exhibit R-2A, RDT&E Project Justification: PB 2020 Defense Advanced Research Projects Agency | | Date: March 2019 |
|---|---|---|
| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-01 / *ELECTRONIC TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| development activities will leverage recent advances in low power, application specific integrated circuit (ASIC) electronics and low power sensors from the internet of things (IoT) community to increase the functionality of microrobotic platforms while increasing platform mobility, maneuverability, and dexterity. The microrobotic platform capabilities enabled by SHRIMP will provide the DoD with significantly more access and capability to operate in small spaces that are practically inaccessible to today's state-of-the-art robotic platforms. Such capability will have impact in search and rescue, disaster relief, infrastructure inspection, and equipment maintenance, among other operations. Foundational research efforts are funded in PE 0601101E, Project ES-01.<br><br>***FY 2019 Plans:***<br>- Initiate development of tethered microrobotic platforms with emphasis on program metrics for size, weight, and duration of operation.<br>***FY 2020 Plans:***<br>- Demonstrate tethered microrobotic platforms meeting program metrics on size, weight, and duration of operation.<br>- Initiate development of an untethered microrobotic platform with an emphasis on size, weight, and performance.<br>***FY 2019 to FY 2020 Increase/Decrease Statement:***<br>The FY 2020 increase reflects the program shifting from initial development to demonstration of tethered microrobotic platforms. | | | |
| ***Title:*** Intelligent Spectroscopic & Temporal Fusion (INSPECT)<br><br>***Description:*** The Intelligent Spectroscopic & Temporal Fusion (INSPECT) program will add relevant spectral content to broadband infrared (IR) imagers to enhance battlefield detection and discrimination while maintaining situational awareness. The resulting desired capability is analogous to human vision that relies upon shape, brightness, and color to recognize and identify objects of interest. Currently fielded systems are either broadband infrared sensors that rely on shape and brightness to identify targets or hyperspectral sensors that rely on color to identify targets. INSPECT will (1) leverage read-out integrated circuits currently in development combined with advances in electrically tunable optical filters and micro-optical components to demonstrate hardware that simultaneously provides situational awareness and target spectral characteristics, and (2) develop intelligent processing for mission-specific band selection. This will enable new applications in passive seeker technology for missiles, battlefield chemical sensing, laser weapon identification and protection, and low probability of detection multi-spectral optical communications.<br><br>***FY 2020 Plans:***<br>- Develop preliminary architecture for use with existing broadband imaging hardware.<br>- Develop preliminary algorithms that provide intelligent band selection.<br>- Begin initial design integration using INSPECT framework.<br>***FY 2019 to FY 2020 Increase/Decrease Statement:*** | - | - | 12.000 |

| Exhibit R-2A, RDT&E Project Justification: PB 2020 Defense Advanced Research Projects Agency | | Date: March 2019 |
|---|---|---|
| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-01 / *ELECTRONIC TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| The FY 2020 increase reflects program initiation. | | | |
| ***Title:*** Instinctual RF | - | - | 11.200 |
| ***Description:*** The Instinctual RF program will develop radio frequency (RF) front-end technology that can protect wideband digital radios against external electromagnetic threats and self-interference, through tunable filtering, limiting, or signal cancellation. Today's multi-function phased arrays that cover broad bandwidth are open to all frequencies with little or no RF filtering. This is due to a lack of reconfigurable filtering that is small enough to integrate into the arrays, limiting the use of wideband multi-function arrays in contested environments. The ability to create reconfigurable bandpass and bandstop filters in the range of 2-18 GHz will be important to implementing transmit/receive modules in next generation multi-function arrays. Another important area of interference mitigation is self-interference. Specifically, in electronic warfare, it would be advantageous to be able to listen while jamming. Instinctual RF will develop the signal cancellation devices that will listen to the transmit signal and subtract the interfering signal from the input of the receiver so that it will be able to hear faint signals near the noise floor. Instinctual RF research will provide feedback mechanisms that instinctively correct these problems, much like the nerves of the human body serve to trigger protective action without conscious thought. Whether for self-induced interference or external interference jamming, this program will show the ability to auto-correct and allow for continued operation.<br><br>***FY 2020 Plans:***<br>- Demonstrate new materials, devices and/or circuit architectures that will enable frequency tuning of band pass and band stop filters in chip-scale size for use in next generation multi-function phased arrays.<br>- Demonstrate new materials, devices and/or circuit architectures that will enable cancellation of signal leakage between two adjacent antennas for electronic warfare applications on small platforms.<br><br>***FY 2019 to FY 2020 Increase/Decrease Statement:***<br>The FY 2020 increase reflects program initiation. | | | |
| ***Title:*** Direct On-Chip Digital Optical Synthesis (DODOS) | 13.000 | 3.000 | - |
| ***Description:*** The Direct On-chip Digital Optical Synthesis (DODOS) program will integrate diverse electronic and photonic components to create a compact, robust, and highly-accurate optical frequency synthesizer for various mission-critical DoD applications. Frequency synthesis and accurate control of radiofrequency and microwave radiation is the enabling technology for radar, satellite and terrestrial communications, positioning and navigation technology, and many other core DoD capabilities. Frequency synthesis and control of light or optical waves, however, has been constrained to laboratory experiments due to the size, fragility, and cost of optical frequency synthesizers. DODOS will leverage recent developments in the field of integrated photonics to enable the development of a ubiquitous, low-cost optical frequency synthesizers. The program could lead to disruptive DoD capabilities, including high-bandwidth optical communications, higher performance Light Detection And Ranging | | | |

| Exhibit R-2A, RDT&E Project Justification: PB 2020 Defense Advanced Research Projects Agency | | Date: March 2019 |
|---|---|---|
| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-01 / *ELECTRONIC TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| (LiDAR), portable high-accuracy atomic clocks, and high-resolution detection of chemical/biological threats at a distance. Basic research for this program is funded within PE 0601101E, Project ES-01.<br><br>***FY 2019 Plans:***<br>- Demonstrate operation of multiple photonic chips in initial synthesizer prototype.<br>- Characterize and deliver multiple DODOS prototypes comprising co-integrated optical frequency synthesizer and control electronics.<br>- Demonstrate a low-noise microwave frequency synthesizer using DODOS components.<br><br>***FY 2019 to FY 2020 Increase/Decrease Statement:***<br>The FY 2020 decrease reflects program completion. | | | |
| ***Title:*** Common Heterogeneous integration & IP reuse Strategies (CHIPS)<br><br>***Description:*** The Common Heterogeneous integration & IP reuse Strategies (CHIPS) program aims to develop the design tools and integration standards required to better leverage leading-edge commercial sector technologies in DoD systems. The program aims to realize modular Integrated Circuits (ICs) that integrate designs using different commercial suppliers and silicon technologies. CHIPS will therefore pursue standardized interfaces for integrating a variety of Intellectual Property (IP) blocks in the form of prefabricated chiplets. The chiplets could be reused across applications, manufacturers, and transistor types, allowing DoD to amortize IC design costs across programs, better align electronics design and fabrication with military performance goals, and expand beyond its traditional reliance on the proprietary capabilities of a few on-shore manufacturers. The CHIPS program moves to Project ELT-02, Beyond Scaling Technologies, in FY 2019. | 28.250 | - | - |
| ***Title:*** Near Zero Energy RF and Sensor Operations (N-ZERO)<br><br>***Description:*** The Near Zero Power RF and Sensor Operations (N-ZERO) program will develop and demonstrate the technologies required to extend the lifetimes of remotely-deployed sensors from months to years. Today's state-of-the-art sensors can be pre-placed and remain dormant until awoken by an external trigger or stimulus. However, the active electronics that monitor for external triggers consume power, limiting sensor lifetimes to between weeks and months. N-ZERO seeks to replace these electronics with passive or extremely low-power devices that continuously monitor the environment and wake up active electronics upon detection of a specific trigger. This would eliminate or significantly reduce standby power consumption, ensuring that sensor lifetimes are limited only by the power required to process and communicate confirmed events. In doing so, N-ZERO could enable wireless sensors with drastically increased mission life and help meet DoD's unfulfilled need for a persistent, event-driven sensing capability. N-ZERO's applied research component will focus on developing radio frequency (RF) communications and physical sensor systems that use energy from an external trigger to collect, process, and detect useful information while rejecting spurious signals and noise. The N-ZERO program moves to Project ELT-02, Beyond Scaling Technologies, in FY 2019. | 20.000 | - | - |

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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-01 / *ELECTRONIC TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| ***Title:*** Circuit Realization At Faster Timescales (CRAFT)<br><br>***Description:*** The Circuit Realization At Faster Timescales (CRAFT) program will develop novel integrated circuit (IC) design flows to reduce by ten times the design and verification effort required for high-performance military electronics. CRAFT will also reduce barriers to the design and fabrication of custom ICs in leading-edge complementary metal oxide semiconductor (CMOS) technology. When selecting electronics for advanced systems, DoD currently must choose between high-performing custom ICs that take years to design and verify or significantly lower-performing general purpose ICs that can be implemented in a few months. The need to protect sensitive IC information further limits DoD's ability to access certain leading-edge commercial electronics. To reduce the design and verification effort, CRAFT will investigate and leverage novel design flows that utilize recent advances in electronic design automation and software design methodologies. These design flows could reduce the manual labor required to develop and verify custom ICs. CRAFT will also explore increased design reuse and flexibility, which will allow DoD to migrate chip fabrication between different foundries or to more advanced technology nodes. These capabilities can help to ensure that the DoD has multiple potential suppliers for critical ICs and help keep military electronics at the leading edge. The CRAFT program moves to Project ELT-02, Beyond Scaling Technologies, in FY 2019. | 24.430 | - | - |
| ***Title:*** Beyond Scaling - Materials<br><br>***Description:*** The Beyond Scaling - Materials program will demonstrate the integration of novel materials into next-generation logic and memory components. Historically, the DoD had taken the lead in shaping the electronics field through research in semiconductor materials, circuits, and processors. However, as DoD focuses on military-specific components and commercial investments eschew the semiconductor space, U.S. fundamental electronics research is stagnant just as an inflection point in Moore's Law (silicon scaling) is about to occur. This program will pursue potential enhancements in electronics that do not rely on Moore's Law, including research not only into new materials but also into the implications of those materials at the device, algorithm, and packaging levels. Research areas will include heterogeneous integration of multiple materials, "sticky logic" devices that combine elements of computation and memory, and leveraging three-dimensional vertical circuit integration to demonstrate dramatic performance improvements with older silicon technologies. The program aims to demonstrate the manufacturability of functioning switches, memory, and novel computational units in a large-scale system. Previous DARPA work on unconventional computing, integration, and reprogrammable memory give confidence in this approach. Basic research for this program is funded within PE 0601101E, Project ES-02. The Beyond Scaling - Materials program moves to ELT-02, Beyond Scaling Technologies, in FY 2019. | 16.000 | - | - |
| ***Title:*** Beyond Scaling - Design*<br><br>***Description:*** *Formerly part of Beyond Scaling - Architectures and Design | 27.000 | - | - |

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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-01 / *ELECTRONIC TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| The Beyond Scaling - Design will develop and demonstrate the tools required for rapidly designing and deploying specialized circuits. As Moore's Law slows and the nation loses the benefit of free, exponential improvements in electronics cost, speed, and power derived from silicon scaling, the DoD will need to maximize the benefits of available silicon technologies by using design tools that enable circuit specialization. Research efforts will explore technologies and techniques such as intelligent design tools, automated physical layout generation, open-source circuit designs, and complete hardware emulation prior to manufacturing. Further research will also develop tools to create exact representations of outdated hardware in the field and to rapidly, cheaply, and safely upgrade these systems with next-generation electronics. The goal of this program is to reduce the barrier to entry for complex system-on-chip (SoC) designs and to provide a secure pathway for the rapid upgrade of electronics. Advances under this program will demonstrate a new DoD capability to create specialized hardware and provide electronics improvements that do not depend on continued, rapid silicon scaling. Basic research for this program is funded within PE 0601101E, Project ES-02. The Beyond Scaling - Design program moves to Project ELT-02, Electronic Technology, in FY 2019. | | | |
| ***Title:*** Beyond Scaling - Architectures*<br>***Description:*** *Formerly part of Beyond Scaling - Architectures and Design<br><br>The Beyond Scaling - Architectures program will demonstrate a new DoD capability to create and utilize specialized hardware by enabling the writing of a common code base on top of customized hardware. The program will explore technologies and techniques such as new domain-specific circuit architectures; co-design of electronics hardware and software; intelligent edge sensors; hardware security architectures; and tight integration of chip-scale processing blocks and artificial intelligence-enabled processing controllers. Basic research for this program is funded within PE 0601101E, Project ES-02. The Beyond Scaling - Architectures program moves to Project ELT-02, Electronic Technology, in FY 2019. | 22.000 | - | - |
| **Accomplishments/Planned Programs Subtotals** | 283.180 | 115.208 | 135.882 |

**C. Other Program Funding Summary ($ in Millions)**

N/A

**Remarks**

**D. Acquisition Strategy**

N/A

**E. Performance Metrics**

Specific programmatic performance metrics are listed above in the program accomplishments and plans section.

| Exhibit R-2A, RDT&E Project Justification: PB 2020 Defense Advanced Research Projects Agency | | | Date: March 2019 |
|---|---|---|---|
| Appropriation/Budget Activity<br>0400 / 2 | R-1 Program Element (Number/Name)<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | Project (Number/Name)<br>ELT-02 / *BEYOND SCALING TECHNOLOGY* | |

| COST ($ in Millions) | Prior Years | FY 2018 | FY 2019 | FY 2020 Base | FY 2020 OCO | FY 2020 Total | FY 2021 | FY 2022 | FY 2023 | FY 2024 | Cost To Complete | Total Cost |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ELT-02: *BEYOND SCALING TECHNOLOGY* | - | 0.000 | 233.639 | 196.310 | - | 196.310 | 192.700 | 203.900 | 204.210 | 204.210 | - | - |

**A. Mission Description and Budget Item Justification**

The Beyond Scaling Technology project recognizes that, within the next decade, the continuous pace of improvements in electronics performance will face the fundamental limits of silicon technology. These limits present a barrier that must be overcome in order for progress to continue. This project will therefore pursue potential electronics performance advancements that do not rely on Moore's Law but instead leverage circuit specialization, to include materials, architectures, and designs intended to suit a specific need. In addition, the Beyond Scaling Technology Project recognizes that the envisioned electronics specialization will require proper security safeguards. Electronics advancements must simultaneously make progress in performance and secure the foundation on which our digital infrastructure relies. Programs within the Beyond Scaling project will look at reducing barriers to making specialized circuits in today's silicon hardware and significantly increase the ease with which DoD can design, deliver, and eventually upgrade critical, customized electronics. Programs will also explore alternatives to traditional circuit architectures, for instance by exploiting vertical circuit integration to optimize electronic devices and by incorporating novel materials, and explore techniques for securing DoD and commercial data and hardware. This project aggregates and continues Beyond Scaling programs that were initiated in PEs/Projects 0602716E/ELT-01 and 0602303E/ IT-02 and IT-03.

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| ***Title:*** Beyond Scaling - Materials | - | 44.349 | 46.000 |
| ***Description:*** The Beyond Scaling - Materials program will demonstrate the integration of novel materials into next-generation logic and memory components. Historically, the DoD had taken the lead in shaping the electronics field through research in semiconductor materials, circuits, and processors. However, as DoD focuses on military-specific components and commercial investments eschew the semiconductor space, U.S. fundamental electronics research is stagnant just as an inflection point in Moore's Law (silicon scaling) is about to occur. This program will pursue potential enhancements in electronics that do not rely on Moore's Law, including research not only into new materials but also into the implications of those materials at the device, algorithm, and packaging levels. Research areas will include heterogeneous integration of multiple materials, "sticky logic" devices that combine elements of computation and memory, and leveraging three-dimensional vertical circuit integration to demonstrate dramatic performance improvements with older silicon technologies. The program aims to demonstrate the manufacturability of functioning switches, memory, and novel computational units in a large-scale system. Previous DARPA work on unconventional computing, integration, and reprogrammable memory give confidence in this approach. Basic research for this program is funded within PE 0601101E, Project ES-02. The Beyond Scaling - Materials program moved from Project ELT-01, Electronic Technology, in FY 2019. | | | |
| ***FY 2019 Plans:***<br>- Demonstrate yield of the first complex three dimensional evaluation circuit. | | | |

| Exhibit R-2A, RDT&E Project Justification: PB 2020 Defense Advanced Research Projects Agency | | Date: March 2019 |
|---|---|---|
| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-02 / *BEYOND SCALING TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| - Release initial design tools to be used for design of three dimensional monolithic circuits.<br>- Demonstrate enhanced yield from circuits using alternative materials fabricated in a 90nm foundry and the ability to scale to larger circuits.<br><br>***FY 2020 Plans:***<br>- Demonstrate fabrication of fully integrated monolithic 3D circuits at a commercial fabrication facility.<br>- Release distribution quality design tools to enable external design of monolithic three dimensional circuits.<br>- Demonstrate large-scale fully functional chips using alternative materials fabricated in a 90 nm foundry with capabilities that are competitive with advanced technology nodes.<br><br>***FY 2019 to FY 2020 Increase/Decrease Statement:***<br>The FY 2020 increase reflects the program transitioning towards demonstrating the ability to take alternative materials through a full commercial process flow. | | | |
| ***Title:*** Beyond Scaling - Architectures* | - | 43.000 | 42.000 |
| ***Description:*** *Formerly part of Beyond Scaling - Architectures and Design<br><br>The Beyond Scaling - Architectures program will demonstrate a new DoD capability to create and utilize specialized hardware by enabling the writing of a common code base on top of customized hardware. The program will explore technologies and techniques such as new domain-specific circuit architectures; co-design of electronics hardware and software; intelligent edge sensors; hardware security architectures; and tight integration of chip-scale processing blocks and artificial intelligence-enabled processing controllers. Basic research for this program is funded within PE 0601101E, Project ES-02. The Beyond Scaling - Architectures program moved from Project ELT-01, Electronic Technology, in FY 2019.<br><br>***FY 2019 Plans:***<br>- Demonstrate that a hardware scheduler will allow for the optimal routing on a specialized integrated circuit in situ of operation.<br>- Initiate design of system-on-chips (SOCs) with heterogeneous mix of processors and algorithm accelerators to solve domain-specific compute problems with good power and performance.<br>- Initiate reconfigurable architecture development and diverse data flow management scheme.<br>- Initiate the definition of a software development environment to enable co-design of reconfigurable hardware.<br><br>***FY 2020 Plans:***<br>- Demonstrate ability to emulate a specialized processor capable of efficiently executing two simultaneous applications.<br>- Demonstrate initial reconfigurable architecture simulation and emulation environment that will drive hardware design decisions and definitions. | | | |

| Exhibit R-2A, RDT&E Project Justification: PB 2020 Defense Advanced Research Projects Agency | | Date: March 2019 |
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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-02 / *BEYOND SCALING TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| - Advance the software tools, development technologies, and design methodologies for SOCs with heterogeneous components that can be easily reprogrammed for specialized applications.<br>- Develop version two of programming languages and compilers that optimize software and hardware at runtime for reconfigurable processors.<br>- Implement an interconnect architecture for a single common embedded bus with the ability to physically isolate high risk transactions and enforce data security and privacy.<br>- Demonstrate 100Mbps sustained throughput across a two-level security architecture and integrate sensitive data isolation techniques into an application relevant to DoD systems.<br>***FY 2019 to FY 2020 Increase/Decrease Statement:***<br>The FY 2020 decrease reflects minor program repricing. | | | |
| ***Title:*** Beyond Scaling - Design*<br>***Description:*** *Formerly part of Beyond Scaling - Architectures and Design<br><br>The Beyond Scaling - Design will develop and demonstrate the tools required for rapidly designing and deploying specialized circuits. As Moore's Law slows and the nation loses the benefit of free, exponential improvements in electronics cost, speed, and power derived from silicon scaling, the DoD will need to maximize the benefits of available silicon technologies by using design tools that enable circuit specialization. Research efforts will explore technologies and techniques such as intelligent design tools, automated physical layout generation, open-source circuit designs, and complete hardware emulation prior to manufacturing. Further research will also develop tools to create exact representations of outdated hardware in the field and to rapidly, cheaply, and safely upgrade these systems with next-generation electronics. The goal of this program is to reduce the barrier to entry for complex system-on-chip (SoC) designs and to provide a secure pathway for the rapid upgrade of electronics. Advances under this program will demonstrate a new DoD capability to create specialized hardware and provide electronics improvements that do not depend on continued, rapid silicon scaling. Rapid design and deployment techniques developed will also consider the need to incorporate security into DoD hardware. Basic research for this program is funded within PE 0601101E, Project ES-02. The Beyond Scaling - Design program moved from Project ELT-01, Electronic Technology, in FY 2019.<br><br>***FY 2019 Plans:***<br>- Determine standards and requirements for interfacing between multiple software modules that will enable the creation of a unified software platform capable of integrating intelligence and learning.<br>- Release an alpha version of the hardware design platform that demonstrates automation within individual software modules, and complete initial evaluation by program collaborators to identify major bugs.<br>- Complete initial design of mixed signal open source Intellectual Property (IP) and gather feedback on IP from government and program users. | - | 33.000 | 40.000 |

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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-02 / *BEYOND SCALING TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| - Finalize standards required to interface between multiple verification modules and demonstrate initial functionality of verification software against a small set of benchmark mixed signal circuits.<br><br>***FY 2020 Plans:***<br>- Deliver software for physical layout of integrated circuits, packages and boards that is 100% automated and achieves 50% power, performance and area compared to traditional best in class techniques.<br>- Demonstrate fabrication of circuits generated from high-level schematics using a fully automated intelligent design flow.<br>- Publically release open source IP modules developed in the program and demonstrate portability between multiple technology nodes.<br>- Publically release a hardware verification platform with functionality evaluated through simulation and emulation of a comprehensive set of digital and mixed signal circuits<br>- Complete an early software release of an emulation flow capable of emulating a small subsystem.<br>- Create an initial testbed to demonstrate accuracy and performance of digital systems designed through hardware emulation to illustrate the reduction of design time and cost.<br>- Define security levels and metrics and establish on-chip and off-chip security infrastructures based on known chip vulnerabilities.<br>- Identify demonstration platforms and develop interface standards for processors that won't reveal manufacturing vulnerabilities using manufacturing and other techniques to enhance security in a secure design flow.<br><br>***FY 2019 to FY 2020 Increase/Decrease Statement:***<br>The FY 2020 increase reflects the transition from initial design and development to the delivery of functional tools, software, intellectual property, and fabricated hardware. | | | |
| ***Title:*** Common Heterogeneous integration & IP reuse Strategies (CHIPS) | - | 15.500 | 17.800 |
| ***Description:*** The Common Heterogeneous integration & IP reuse Strategies (CHIPS) program aims to develop the design tools and integration standards required to better leverage leading-edge commercial sector technologies in DoD systems. The program aims to realize modular Integrated Circuits (ICs) that integrate designs using different commercial suppliers and silicon technologies. CHIPS will therefore pursue standardized interfaces for integrating a variety of Intellectual Property (IP) blocks in the form of prefabricated chiplets. The chiplets could be reused across applications, manufacturers, and transistor types, allowing DoD to amortize IC design costs across programs, better align electronics design and fabrication with military performance goals, and expand beyond its traditional reliance on the proprietary capabilities of a few on-shore manufacturers. The CHIPS program moved from Project ELT-01, Electronic Technology, in FY 2019.<br><br>***FY 2019 Plans:***<br>- Complete module design activities to determine performance and program benefits of new processes enabled by the program. | | | |

| Exhibit R-2A, RDT&E Project Justification: PB 2020 Defense Advanced Research Projects Agency | | Date: March 2019 |
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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-02 / *BEYOND SCALING TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| - Initiate fabrication of approved modules to determine performance and program benefits of new processes enabled by the program.<br>- Continue the study of the system level impact of IP re-use for the optimal use of digital functional blocks.<br>***FY 2020 Plans:***<br>- Complete module fabrication and testing to demonstrate functionality of the CHIPS interface and chiplets in representative applications.<br>- Initiate design of upgraded modules to determine performance and program benefits of new processes enabled by the program.<br>- Complete the study of the system level impact of IP re-use for the optimal use of digital functional blocks.<br>***FY 2019 to FY 2020 Increase/Decrease Statement:***<br>The FY 2020 increase reflects the program shifting from module design to module fabrication. | | | |
| ***Title:*** System Security Integrated Through Hardware and firmware (SSITH) | - | 22.790 | 19.000 |
| ***Description:*** The System Security Integrated Through Hardware and firmware (SSITH) program seeks to secure DoD and commercial electronic systems against cybersecurity threats by developing novel hardware/firmware security architectures and hardware design methodologies. Current responses to cybersecurity attacks typically consist of developing and deploying software patches to address specific vulnerabilities in a software firewall without addressing potential vulnerabilities in the underlying hardware architecture. To address this challenge, SSITH will drive new research in electronics hardware security and exploit current research in areas such as cryptographic-based computing and hardware verification. Implementation of these advanced ideas has been enabled by the extremely capable semiconductor technology driven by Moore's Law. The program will also investigate flexible hardware architectures that adapt to and limit the impact of new cybersecurity attacks. Finally, SSITH will seek to mitigate the potential negative impact of new security protection architectures on system performance and power usage. Once developed, SSITH capabilities will be applicable to both commercial and military electronic systems. The SSITH program moved from Project IT-03, Information Assurance and Survivability, in FY 2019.<br>***FY 2019 Plans:***<br>- Implement new hardware architectures on Field-Programmable Gate Array (FPGA) demonstration platforms that demonstrate scalable, flexible, and robust protection against external attacks on embedded and mobile processing hardware.<br>- Utilize simulation and hardware emulation to confirm the expected improvement in protection of the new hardware architectures relative to current software only protection.<br>- Evaluate SSITH security approaches through independent Red Team attack on the security architectures as implemented on FPGA hardware.<br>***FY 2020 Plans:*** | | | |

| Exhibit R-2A, RDT&E Project Justification: PB 2020 Defense Advanced Research Projects Agency | | Date: March 2019 |
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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-02 / *BEYOND SCALING TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| - Implement new hardware architectures on FPGA demonstration platforms that demonstrate scalable, flexible, and robust protection against external attacks on high-performance, out-of-order processing hardware.<br>- Develop distribution-ready design tools to implement SSITH hardware protection methods in new hardware.<br>- Utilize simulation and emulation to evaluate the tradeoffs between security, power, and performance of hardware.<br>- Formalize security metrics and establish a clear distribution mechanism for those metrics.<br>***FY 2019 to FY 2020 Increase/Decrease Statement:***<br>The FY 2020 decrease reflects the program transitioning from implementing hardware design to testing hardware. | | | |
| ***Title:*** Hierarchical Identify Verify Exploit (HIVE) | - | 17.600 | 16.510 |
| ***Description:*** The Hierarchical Identify Verify Exploit (HIVE) program will pursue new hardware architectures and algorithms for improving the efficiency of graph and sparse data analytics. When developing operationally significant intelligence, human analysts today are forced to reduce the scope of the problems that they can address and the tempo of their analyses due to the limitations of currently deployed hardware. Because of these limitations the amount of information gathered is quickly outstripping the human ability to review, process, fuse, and interpret. To resolve this challenge, HIVE seeks to leverage improvements in computational efficiency to augment the analyst's ability to integrate large streams of data. The program will investigate advances in chip architecture and data analytics algorithms that can allow machines to infer meaning out of data based on the information needs of the warfighter. Program success would therefore enable the warfighter to understand far more of the battlespace in real time. The HIVE program moved from Project IT-02, High Productivity, High Performance Responsive Architectures, in FY 2019.<br>***FY 2019 Plans:***<br>- Improve the toolsets based on information gathered from previous testing and deliver a beta version of the software.<br>- Expand the code sets and code set analysis for final detailed power and performance analysis.<br>- Develop initial full architectural design and detailed performance analysis to drive final design decisions.<br>- Demonstrate that HIVE can run DoD problem sets on field programmable gate arrays (FPGAs) which emulate the HIVE chip and measure both power and performance improvements of the proposed architectures.<br>***FY 2020 Plans:***<br>- Complete development of the FPGA emulator and porting of government workflows.<br>- Finalize the HIVE chip architecture and deliver design for fabrication.<br>- Complete application programming interface for HIVE runtime environment.<br>***FY 2019 to FY 2020 Increase/Decrease Statement:*** | | | |

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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-02 / *BEYOND SCALING TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| The FY 2020 decrease is the result of development work on architectural design concluding and focusing on delivering final design for fabrication. | | | |
| ***Title:*** Digital RF Battlespace Emulator (DRBE) | - | 8.000 | 15.000 |
| ***Description:*** The Digital RF Battlespace Emulator (DRBE) program aims to develop a large-scale, interactive, emulated radiofrequency (RF) environment, providing the DoD with much needed capability to cost-effectively evaluate adaptive, intelligent, and spatially distributed next-generation RF systems. Current U.S. test infrastructure is no longer able to successfully exercise RF systems in relevant environments, which should account for hundreds of DoD systems coordinating against hundreds of adversary systems. Due to the critical dependency of nearly all platforms and missions on the RF spectrum and the increasingly advanced RF capabilities of peer adversaries, current infrastructure limitations represent a critical capability gap. Existing test approaches are either: 1) small-scale laboratory tests under well controlled but unrealistic conditions or 2) massive training exercises, which occur at most annually due to the required cost and manpower and do not fully collect necessary data. To overcome these limitations, DRBE will leverage advances in massively multi-core computing hardware and high-bandwidth digital cross connects to emulate realistic RF environments that account for RF platform movement, signal propagation effects and delays, signal interference, and interactions between RF systems. The electronics architecture which supports these goals is beyond anything that exists today, based on the power and latency requirements that this emulation environment demands. DRBE will pursue three technical thrust areas: architecture, massively multi-core computing, and scenario modeling. The resulting test environment should allow plug-and-play connections for hundreds of RF systems in a 100 km battlespace test. Multi-system exercises could then be quickly executed through many different combat scenarios and variations. DRBE should therefore serve to develop CONOPS, inform battle plans, and fine-tune the performance of both individual and large groups of RF systems.<br><br>***FY 2019 Plans:***<br>- Conduct architecture scaling analysis to define a solution supporting hundreds of RF systems.<br>- Demonstrate basic physical building blocks that will be able to handle the immense throughput expected.<br><br>***FY 2020 Plans:***<br>- Complete first-generation DRBE system design.<br>- Emulate first-generation DRBE system performance using non-real-time software.<br>- Begin fabrication of a first-generation DRBE system.<br>- Begin development and testing of second-generation DRBE basic physical building blocks.<br><br>***FY 2019 to FY 2020 Increase/Decrease Statement:***<br>The FY 2020 increase reflects the program shifting from design to beginning fabrication of the DRBE system. | | | |
| ***Title:*** Circuit Realization At Faster Timescales (CRAFT) | - | 9.400 | - |

| Exhibit R-2A, RDT&E Project Justification: PB 2020 Defense Advanced Research Projects Agency | | Date: March 2019 |
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| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-02 / *BEYOND SCALING TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| ***Description:*** The Circuit Realization At Faster Timescales (CRAFT) program will develop novel integrated circuit (IC) design flows to reduce by ten times the design and verification effort required for high-performance military electronics. CRAFT will also reduce barriers to the design and fabrication of custom ICs in leading-edge complementary metal oxide semiconductor (CMOS) technology. When selecting electronics for advanced systems, DoD currently must choose between high-performing custom ICs that take years to design and verify or significantly lower-performing general purpose ICs that can be implemented in a few months. The need to protect sensitive IC information further limits DoD's ability to access certain leading-edge commercial electronics. To reduce the design and verification effort, CRAFT will investigate and leverage novel design flows that utilize recent advances in electronic design automation and software design methodologies. These design flows could reduce the manual labor required to develop and verify custom ICs. CRAFT will also explore increased design reuse and flexibility, which will allow DoD to migrate chip fabrication between different foundries or to more advanced technology nodes. The CRAFT program moved from Project ELT-01, Electronic Technology, in FY 2019.<br><br>***FY 2019 Plans:***<br>- Complete the fourth multi-project wafer shuttle run utilizing the final CRAFT design flows.<br>- Finalize the design vault to facilitate access to the CRAFT design flow and related IP for DoD use.<br>- Utilize design flow and intellectual property (IP) from CRAFT to complete DoD reference designs.<br><br>***FY 2019 to FY 2020 Increase/Decrease Statement:***<br>The FY 2020 decrease reflects program completion. | | | |
| ***Title:*** Near Zero Energy RF and Sensor Operations (N-ZERO) | - | 10.000 | - |
| ***Description:*** The Near Zero Power RF and Sensor Operations (N-ZERO) program will develop and demonstrate the technologies required to extend the lifetimes of remotely-deployed sensors from months to years. Today's state-of-the-art sensors can be pre-placed and remain dormant until awoken by an external trigger or stimulus. However, the active electronics that monitor for external triggers consume power, limiting sensor lifetimes to between weeks and months. N-ZERO seeks to replace these electronics with passive or extremely low-power devices that continuously monitor the environment and wake up active electronics upon detection of a specific trigger. This would eliminate or significantly reduce standby power consumption, ensuring that sensor lifetimes are limited only by the power required to process and communicate confirmed events. In doing so, N-ZERO could enable wireless sensors with drastically increased mission life and help meet DoD's unfulfilled need for a persistent, event-driven sensing capability. N-ZERO's applied research component will focus on developing radio frequency (RF) communications and physical sensor systems that use energy from an external trigger to collect, process, and detect useful information while rejecting spurious signals and noise. A basic research component is budgeted under PE 0601101E, Project ES-01. The N-ZERO program moved from Project ELT-01, Electronics Technology, in FY 2019. | | | |

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|---|---|---|
| **Appropriation/Budget Activity**<br>0400 / 2 | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* | **Project (Number/Name)**<br>ELT-02 / *BEYOND SCALING TECHNOLOGY* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2018 | FY 2019 | FY 2020 |
|---|---|---|---|
| ***FY 2019 Plans:***<br>- Design, implement and test signal processing to improve the detection and classification capabilities of N-ZERO sensor systems in the presence of significant background interference.<br>- Facilitate transition opportunities for microsystems enabling passive or near zero energy collection, processing and detection of RF communications and physical sensor signatures at reduced signal strength.<br>- Continue the development of near zero power wireless wake-up sensors for health monitoring of high-value machinery for aerospace applications.<br>***FY 2019 to FY 2020 Increase/Decrease Statement:***<br>The FY 2020 decrease reflects program completion. | | | |
| **Accomplishments/Planned Programs Subtotals** | - | 203.639 | 196.310 |

| | FY 2018 | FY 2019 |
|---|---|---|
| ***Congressional Add:*** DARPA Electronics Resurgence Initiative | - | 30.000 |
| ***FY 2019 Plans:*** - Initiate or enhance ongoing efforts to demonstrate electronics that can enforce security and privacy protections for electronics components critical to DoD overmatch capabilities.<br>- Confirm, via emulation and physical demonstration, that DARPA-developed hardware security technologies can improve the protection of hardware architectures and national critical infrastructure.<br>- Complete abstractions for the physical design of cryptographic hardware intellectual property for use in critical DoD applications.<br>- Incorporate techniques for the physical isolation of sensitive data processing transactions into an application associated with an ongoing DoD program. | | |
| **Congressional Adds Subtotals** | - | 30.000 |

**C. Other Program Funding Summary ($ in Millions)**

N/A

**Remarks**

**D. Acquisition Strategy**

N/A

**E. Performance Metrics**

Specific programmatic performance metrics are listed above in the program accomplishments and plans section.