Exhibit R-2, RDT&E Budget Item Justification: PB 2019 Defense Advanced Research Projects Agency	Date: February 2018
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*

COST ($ in Millions)	Prior Years	FY 2017	FY 2018	FY 2019 Base	FY 2019 OCO	FY 2019 Total	FY 2020	FY 2021	FY 2022	FY 2023	Cost To Complete	Total Cost
Total Program Element	-	190.624	295.447	333.847	-	333.847	307.073	344.283	364.773	381.683	-	-
ELT-01: *ELECTRONIC TECHNOLOGY*	-	190.624	295.447	141.647	-	141.647	116.623	152.673	172.373	188.973	-	-
ELT-02: *BEYOND SCALING TECHNOLOGY*	-	0.000	0.000	192.200	-	192.200	190.450	191.610	192.400	192.710	-	-

A. Mission Description and Budget Item Justification

The Electronics Technology Program Element is budgeted in the Applied Research Budget Activity because its objective is to develop electronics that make a wide range of military applications possible. The Electronics Technology Project focuses on turning basic advancements into the underpinning technologies required to address critical national security issues and to enable an information-driven warfighter.

Advances in microelectronic device technologies continue to significantly benefit improved weapons effectiveness, intelligence capabilities, and information superiority. The Electronic Technology project therefore supports continued advancement in microelectronics, including electronic and optoelectronic devices, Microelectromechanical Systems (MEMS), semiconductor device design and fabrication, and new materials and material structures. Particular focuses of this work include reducing the barriers to designing and fabricating custom electronics and exploiting improved manufacturing techniques to provide low-cost, high-performance sensors. Programs in this project will also greatly improve the size, weight, power, and performance characteristics of electronic systems; support positioning, navigation, and timing in GPS-denied environments; and develop sensors more sensitive and robust than today's standards.

The Electronic Technology project will also investigate the feasibility, design, and development of powerful devices, including non-silicon-based materials technologies to achieve low-cost, reliable, fast, and secure computing, communication, and storage systems. Rapid design and utilization of these new technologies will be a critical focus of ELT-01, as DoD looks for mechanisms to speed the development and fielding of advanced technologies.

This project has six major focus areas: Electronics, Photonics, MicroElectroMechanical Systems, Architectures, Algorithms, and other Electronic Technology research.

The Beyond Scaling Technology project recognizes that phenomenal advancements in electronics will face the fundamental limits of silicon technology in the early 21st century, presenting a barrier that must be overcome in order for progress to continue. This project will therefore pursue potential electronics performance advancements that do not rely on Moore's Law but instead leverage circuit specialization, to include leveraging materials, architectures, and designs that are designed to suit a specific need. Programs within the Beyond Scaling Technology project will look at reducing barriers to making specialized circuits in today's silicon hardware. They will also explore alternatives to traditional circuit architectures, for instance by exploiting chip-scale heterogeneous integration of differing material technologies, using "sticky logic" devices that combine computation and memory functions, and vertical circuit integration to optimize electronic devices. This Project is not a new start. It aggregates and continues Beyond Scaling programs that were initiated in PEs/Projects 0602716E/ELT-01 and 0602303E/IT-02 and IT-03.

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B. Program Change Summary ($ in Millions)	FY 2017	FY 2018	FY 2019 Base	FY 2019 OCO	FY 2019 Total
Previous President's Budget	221.911	295.447	234.685	-	234.685
Current President's Budget	190.624	295.447	333.847	-	333.847
Total Adjustments	-31.287	0.000	99.162	-	99.162
• Congressional General Reductions	-15.000	0.000			
• Congressional Directed Reductions	0.000	0.000			
• Congressional Rescissions	0.000	0.000			
• Congressional Adds	0.000	0.000			
• Congressional Directed Transfers	0.000	0.000			
• Reprogrammings	-6.110	0.000			
• SBIR/STTR Transfer	-10.177	0.000			
• TotalOtherAdjustments	-	-	99.162	-	99.162

Change Summary Explanation

FY 2017: Decrease reflects Congressional reduction, reprogrammings and the SBIR/STTR transfer.

FY 2018: N/A

FY 2019: Increase reflects expanded focus in the Beyond Scaling Technology Project supporting the Electronics Resurgence Initiative (ERI) offset by decreases in Electronic Technology.

Exhibit R-2A, RDT&E Project Justification: PB 2019 Defense Advanced Research Projects Agency			Date: February 2018
Appropriation/Budget Activity 0400 / 2	R-1 Program Element (Number/Name) PE 0602716E / *ELECTRONICS TECHNOLOGY*	Project (Number/Name) ELT-01 / *ELECTRONIC TECHNOLOGY*	

COST ($ in Millions)	Prior Years	FY 2017	FY 2018	FY 2019 Base	FY 2019 OCO	FY 2019 Total	FY 2020	FY 2021	FY 2022	FY 2023	Cost To Complete	Total Cost
ELT-01: *ELECTRONIC TECHNOLOGY*	-	190.624	295.447	141.647	-	141.647	116.623	152.673	172.373	188.973	-	-

A. Mission Description and Budget Item Justification

The Electronics Technology Program Element is budgeted in the Applied Research Budget Activity because its objective is to develop electronics that make a wide range of military applications possible. The Electronics Technology Project focuses on turning basic advancements into the underpinning technologies required to address critical national security issues and to enable an information-driven warfighter.

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The Electronic Technology project will also investigate the feasibility, design, and development of powerful devices, including non-silicon-based materials technologies to achieve low-cost, reliable, fast, and secure computing, communication, and storage systems. Rapid design and utilization of these new technologies will be a critical focus of ELT-01, as DoD looks for mechanisms to speed the development and fielding of advanced technologies.

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
Title: High power Amplifier using Vacuum electronics for Overmatch Capability (HAVOC)	13.000	18.000	11.803
Description: The High power Amplifier using Vacuum electronics for Overmatch Capability (HAVOC) program seeks to develop compact Radio Frequency (RF) signal amplifiers for air, ground, and ship-based communications and sensing systems. HAVOC amplifiers would enable these systems to access the high-frequency millimeter-wave portion of the Electromagnetic (EM) spectrum, facilitating increased range and other performance improvements. Today, the effectiveness of combat operations across all domains increasingly depends on DoD's ability to control and exploit the EM spectrum and to deny its use to adversaries. However, the proliferation of inexpensive commercial RF sources has made the EM spectrum crowded and contested, challenging our spectrum dominance. Operating at higher frequencies, such as the millimeter-wave, helps DoD to overcome these issues and offers numerous tactical advantages such as high data-rate communications and high resolution and sensitivity for radar and sensors. Opportunities for transferring HAVOC technology to the Services will be identified during the			

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
execution of the early phases of the program. Technology transfer efforts will follow a spiral development process to mitigate risk and provide the opportunity to incorporate new technological developments as they occur. Basic research for this program is funded within PE 0601101E, Project ES-01. ***FY 2018 Plans:*** - Design, fabricate, and test wide bandwidth vacuum windows with high power handling capability. - Investigate new magnetic materials and magnet configurations that enable compact, integrated beam focusing and transport architectures. - Integrate components into prototype amplifiers and begin testing. ***FY 2019 Plans:*** - Design, fabricate, and test higher power, higher duty cycle devices to meet advanced program metrics. - Research novel techniques and technologies to address greater thermal management requirements of higher power devices. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The decrease in FY 2019 reflects the shift from integration of components to final testing.			
Title: Precise Robust Inertial Guidance for Munitions (PRIGM)	13.624	20.500	14.844
Description: The Precise Robust Inertial Guidance for Munitions (PRIGM) program aims to develop inertial sensor technologies for positioning, navigation, and timing (PNT) in GPS-denied environments. When GPS is not available, these inertial sensors can provide autonomous PNT information. The program will exploit recent advances in integrating photonic (light-manipulating) components into electronics and in employing Microelectromechanical Systems (MEMS) as high-performance inertial sensors for use in extreme environments. Whereas conventional MEMS inertial sensors can suffer from inaccuracies due to factors such as temperature sensitivity, new photonics-based PNT techniques have demonstrated the ability to reject these inaccuracies. PRIGM will focus on two areas. By 2020, it aims to develop and transition a Navigation-Grade Inertial Measurement Unit (NGIMU), a state-of-the-art MEMS device, to DoD platforms. By 2030, it aims to develop Advanced Inertial MEMS Sensors (AIMS) that can provide gun-hard, high-bandwidth, high dynamic range navigation for GPS-free munitions. These advances should enable navigation applications, such as smart munitions, that require low-cost, size, weight, and power inertial sensors with high bandwidth, precision, and shock tolerance. PRIGM will advance state-of-the-art MEMS gyros from TRL-3 devices to a TRL-6 transition platform, eventually enabling the Service Labs to perform TRL-7 field demonstrations. Basic research for this program is funded within PE 0601101E, Project ES-01 and advanced technology development for the program is budgeted in PE 0603739E, Project MT-15. ***FY 2018 Plans:*** - Design and fabricate heterogeneously integrated, chip-scale waveguide optical gyroscopes.			

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
- Demonstrate navigation grade accuracy and stability of integrated inertial sensors. ***FY 2019 Plans:*** - Package all component technology and test photonic-MEMS inertial sensor performance robustness to environmental temperature variation for repeatability between routine operations. - Demonstrate inertial sensor survival and operation through laboratory-representative launch events. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The decrease in FY 2019 reflects completion of design to transition of packaging component technology and testing inertial sensor performance.			
Title: Wafer-scale Infrared Detectors (WIRED) ***Description:*** The WIRED program addresses the need for low-cost, high-performance imaging sensors in the short-wave and mid-wave infrared (SWIR/MWIR) bands. These sensors will provide increased standoff distances for small unmanned aerial vehicles, low-cost missiles, handheld weapon sights and surveillance systems, helmet-mounted systems, and ground-vehicle-mounted threat warning systems. WIRED proposes to manufacture these sensors at the wafer scale, which reduces costs by processing dozens to hundreds of camera imaging arrays at a time. Wafer-scale manufacturing has already driven a revolution in optical imaging in the Long-Wave Infrared Thermal (LWIR) spectrum, with high-resolution digital cameras and LWIR sensors having become commonplace or widely-available. However, no similar technologies exist for the SWIR/MWIR bands. WIRED could therefore drive a similar revolution in SWIR/MWIR. The program aims to significantly reduce the weight and volume of MWIR detectors, which today require heavy cryogenic cooling systems, and increase the resolution of SWIR detectors by dramatically reducing their pixel size relative to the state-of-the-art. ***FY 2018 Plans:*** - Demonstrate improved imaging from MWIR detectors that are integrated directly onto readout integrated circuits (ROICs) and evaluate detector performance/characteristics at temperatures of 250 K. - Demonstrate improved imaging from small pixel SWIR detectors that are integrated directly onto ROICs and evaluate detector performance/characteristics. - Update cost models based on detector performance. - Demonstrate performance of a LWIR device at temperatures of 298 K. ***FY 2019 Plans:*** - Demonstrate an integrated MWIR camera and evaluate performance at temperature of 270 K. - Demonstrate an integrated small-pitch SWIR camera and optimize design of high-resolution SWIR camera.	14.000	19.000	18.500

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
- Demonstrate performance of a LWIR device array and demonstrate improved performance at 298 K. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The decrease in FY 2019 reflects minor program repricing.			
Title: Modular Optical Aperture Building Blocks (MOABB) ***Description:*** The Modular Optical Aperture Building Blocks (MOABB) program aims to greatly improve the cost, size, weight, and performance of free-space optical systems. These systems enable applications such as Light Detection And Ranging (LIDAR), laser communications, laser illumination, navigation, and 3D imaging. Specifically, MOABB will construct millimeter-scale optical building blocks that can be coherently arrayed to form larger, higher power devices. These building blocks would replace the traditional large and expensive precision lenses and mirrors, which require slow mechanical steering, that form conventional optical systems. MOABB will develop scalable optical phased arrays that can steer light waves without the use of mechanical components. These advances would allow for a 100-fold reduction in size and weight and a 1,000-fold increase in the steering rate of optical systems. ***FY 2018 Plans:*** - Demonstrate beam steering using photonic phase shifters and wavelength tuning in low-loss waveguide gratings. - Demonstrate a scalable unit cell with integrated amplification. - Complete preliminary LIDAR system designs. ***FY 2019 Plans:*** - Demonstrate frequency modulated LIDAR functionality of a unit cell. - Coherently combine light between multiple unit cells. - Demonstrate synthesis of multiple light beams generated from a common aperture. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The increase in FY 2019 reflects minor program repricing.	16.911	22.000	23.000
Title: Atomic Clock with Enhanced Stability (ACES) ***Description:*** The Atomic Clock with Enhanced Stability (ACES) program aims to develop extremely stable chip-scale atomic clocks for unmanned aerial vehicles and other low size, weight, and power (SWaP) platforms with extended mission durations. Atomic clocks provide the high-performance backbone of timing and synchronization for DoD navigation; communications; electronic warfare (EW); and intelligence, surveillance, and reconnaissance (ISR) systems. However, atomic clocks are limited, particularly by temperature sensitivity, aging over long timescales, and a loss of accuracy when power cycled. By employing alternative approaches to confining and measuring atomic particles, ACES could yield a 100x - 1000x improvement in key performance parameters related to each of these limitations. ACES will also focus on developing the component technologies	10.589	21.000	18.000

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
necessary for low-cost manufacturing and for deployment in harsh DoD-relevant environments. Among its many benefits, program success could help reduce the risk posed by a growing national dependence on GPS, allowing systems to maintain their timing accuracy in the event of temporary GPS unavailability. ***FY 2018 Plans:*** - Perform laboratory demonstration of functioning ACES clock meeting Phase 1 metrics of power consumption, retrace, and instability. - Design an integrated physics package meeting Phase 2 size, weight, and power (SWaP) objectives. - Initiate fabrication and testing of an integrated physics package meeting the ACES Phase 2 SWaP, retrace, aging, and instability. ***FY 2019 Plans:*** - Complete fabrication and testing of an integrated physics package meeting the ACES Phase 2 SWaP, retrace, aging, and instability goals. - Deliver prototype physics package and supporting electronics to government facility for testing. - Design an integrated physics package meeting Phase 3 SWaP objectives. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The decrease in FY 2019 reflects ACES completing fabrication and conducting final testing for transition to the Service Labs for further development.			
Title: Limits of Thermal Sensors (LOTS)	9.000	9.000	9.000
Description: The Limits of Thermal Sensors (LOTS) program aims to demonstrate long-wave infrared (LWIR) detector technologies with both high performance and low-size, weight, power, and cost (SWaP-C). The resulting technologies would enable improvements in imaging systems such as night-vision goggles, infrared-guided missiles, and missile threat warning systems. Currently, LWIR-enabled systems must choose between large and expensive cryogenically-cooled detectors, which offer high sensitivity and low response times, and uncooled detectors called microbolometers, which offer significant SWaP-C reductions at lower performance. LOTS seeks to develop microbolometers that can compete with larger cameras in terms of higher sensitivity required to detect signals over long ranges and lower response time required to avoid image blur. These technologies will allow DoD to deploy smaller, lighter, and cheaper sensors on critical, high-value assets while maintaining or improving their ability to engage fast-moving or distant targets. ***FY 2018 Plans:*** - Build LWIR cameras using LOTS microbolometer designs and demonstrate 2x improvement over state of the art using the microbolometer figure of merit.			

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
- Test cameras for radiometric performance and sensitivity and deliver camera hardware. ***FY 2019 Plans:*** - Build LWIR cameras with refined sensors to meet final program specifications. - Validate test camera sensitivity and response time in a relevant application environment.			
Title: Direct On-Chip Digital Optical Synthesis (DODOS) ***Description:*** The Direct On-chip Digital Optical Synthesis (DODOS) program will integrate diverse electronic and photonic components to create a compact, robust, and highly-accurate optical frequency synthesizer for various mission-critical DoD applications. Frequency synthesis and accurate control of radiofrequency and microwave radiation is the enabling technology for radar, satellite and terrestrial communications, positioning and navigation technology, and many other core DoD capabilities. Frequency synthesis and control of light or optical waves, however, has been constrained to laboratory experiments due to the size, fragility, and cost of optical frequency synthesizers. DODOS will leverage recent developments in the field of integrated photonics to enable the development of a ubiquitous, low-cost optical frequency synthesizers. The program could lead to disruptive DoD capabilities, including high-bandwidth optical communications, higher performance Light Detection And Ranging (LiDAR), portable high-accuracy atomic clocks, and high-resolution detection of chemical/biological threats at a distance. Basic research for this program is funded within PE 0601101E, Project ES-01. ***FY 2018 Plans:*** - Develop DODOS photonics packaging architectures and deliver prototypes with integrated photonic chips compatible with large-scale batch manufacturing. - Improve the long-term stability of the miniaturized DODOS prototypes and demonstrate synthesizer performance meeting the Phase 2 program goals. ***FY 2019 Plans:*** - Successful field demonstration of co-integrated optical frequency synthesizer and control electronics on the DODOS prototype. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The decrease in FY 2019 reflects final demonstration of the DODOS prototype.	10.000	13.000	6.000
Title: Atomic Magnetometry for Biological Imaging In Earth's Native Terrain (AMBIIENT) ***Description:*** The Atomic Magnetometry for Biological Imaging In Earth's Native Terrain (AMBIIENT) program will develop novel magnetic sensors capable of providing high-sensitivity signal measurements in the presence of ambient magnetic fields. In recent years, the value of magnetic imaging, for example for cardiac and other biological signals, has shown tremendous potential for advanced research and clinical diagnosis. Practical application, however, has been limited. Interference from natural and manmade ambient magnetic fields has required that the measurements be performed in specialized, magnetically-shielded	-	12.000	13.000

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
research facilities. The AMBIIENT program will exploit novel physical architectures that are resistant to the impact of common noise sources. The AMBIIENT sensor itself must be able to detect the gradient of a local magnetic field while subtracting the much larger ambient signal. This would enable low-cost, portable, high-sensitivity measurements for in-the-field applications. In addition to medical research and clinical diagnosis, AMBIIENT sensors promise to enable diverse sensing applications including magnetic gradient navigation, anomaly detection, perimeter monitoring, and Ultralow Frequency (ULF) communications. ***FY 2018 Plans:*** - Develop preliminary architectures for direct gradient sensing of magnetic fields. - Develop and test quantitative models of gradient sensor physics. - Perform laboratory validation of proof-of-principle gradient sensor physics performance. ***FY 2019 Plans:*** - Fabricate and test preliminary architectures for direct gradient sensing of magnetic fields. - Refine quantitative models of gradient sensor physics. - Perform laboratory testing of proof-of-principle gradient sensor physics package meeting AMBIIENT Phase 1 size weight and power, accuracy, and sensitivity goals. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The increase in FY 2019 reflects minor program repricing.			
Title: Dynamic Range-enhanced Electronics and Materials (DREaM) ***Description:*** The Dynamic Range-enhanced Electronics and Materials (DREaM) program aims to develop intrinsically linear (ideal) radio frequency (RF) transistors with improved power efficiency and extremely high dynamic range. Linearity, power efficiency, and dynamic range are fundamental characteristics that allow RF systems to reliably transmit clear signals. Improving these characteristics is essential to operating in a crowded RF environment and to enabling next-generation communication, sensing, and electronic warfare systems. Traditional RF transistor designs typically require a trade-off between linearity and broadcast power, and poor linearity results in undesired interference. DREAM will overcome this tradeoff by employing new transistor materials, architectures, and designs. The resulting DREAM-enabled technologies will allow future RF electronics to increase their operating range without polluting the already-congested RF spectrum and while consuming less system power. ***FY 2018 Plans:*** - Explore novel device structures and emerging materials that will result in high power, high linearity and high power efficiency RF transistors.	-	14.000	18.000

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
- Develop high power and linear power transistor prototype that provides three times more power density and linearity than the state of the art. ***FY 2019 Plans:*** - Develop initial low noise and lower power linear transistor prototype that provides 10 times improvement of linearity figure of merit than the state of the art. - Develop fabrication processes for initial advanced transistor architectures and complete early characterization of RF transistor prototypes with two times improvement in output power over the state of the art. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The increase in FY 2019 reflects the need to fund a more diverse portfolio to facilitate alignment with DoD mission needs and support an increased number of RF transistor prototype deliverables for characterization by the government.			
Title: Wireless Autonomous Vehicle Power Transfer (WAVPT) ***Description:*** The Wireless Autonomous Vehicle Power Transfer (WAVPT) program will develop small footprint, efficient receivers to enable power beaming from a ground-based transmitter to a remote unmanned aerial vehicle (UAV). UAVs are currently powered by large, heavy chemical batteries or an engine, with associated liquid fuel. This consumes a large percentage of the UAV's weight budget and places strict limitations on its range. Wireless power transfer represents a paradigm-changing solution to power distribution by alleviating the need to carry all energy sources on-board, drastically reducing UAV weight, and increasing aircraft endurance. Additional power can also be made available for the UAV's payload, allowing use of higher-functionality sensing and computing systems and enabling better data exploitation and threat response. Previous wireless power transfer experiments have demonstrated delivery of over 30 kilowatts of power over a distance of one kilometer but have seen limited adoption due to the prohibitively large, meter-sized receivers required. WAVPT will leverage recent advances in directed energy sources and beam-forming capabilities and develop new receiver architectures to demonstrate efficient wireless power transfer in a small form-factor. Advanced semiconductor materials and processing techniques will be used to develop low-cost, centimeter-sized receivers with high efficiency and energy densities, enabling integration within a small platform. The program will culminate with a demonstration of hundreds of watts of power being transferred from a ground-based transmitter to a UAV at least one kilometer away. The technology that is developed within this program can break the inherent tradeoff between mission duration and weight for unmanned vehicles and transform next-generation military systems. ***FY 2018 Plans:*** - Devise a detailed Concept of Operations (CONOPs) for wireless power beaming, including selected UAV, dwell time needed for charging, payload power requirements, and platform integration. - Identify link budget for wireless power transfer over one kilometer.	-	9.000	9.500

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
- Demonstrate a proof of concept flight demo using commercial components. ***FY 2019 Plans:*** - Design a custom high-power, high-efficiency, receiver architecture for mission-required beam transmission. - Complete designs and begin component development for a custom integrated wireless power system integrated with a Group 2/3 UAV. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The increase in FY 2019 reflects minor program repricing.			
Title: Arrays at Commercial Timescales (ACT) ***Description:*** The Arrays at Commercial Timescales (ACT) program will develop standardized, fully digital phased array system components to enable rapid upgrades to DoD communications, electronic warfare, and radar systems. Phased arrays, which control and steer radio signals, have helped the DoD maintain technological superiority in nearly every theater of conflict. However, current phased array components are based on custom analog electronics, making them expensive to develop, difficult to upgrade, and time-consuming to deploy. ACT will address this challenge by leveraging programmable, commercial-off-the-shelf, digital components that can undergo yearly technology refreshes in response to a continually changing threat environment. This approach can dramatically reduce the time and cost required to develop and update DoD phased arrays. Further, the ongoing cost reductions and performance improvements typical in the commercial sector could enable the DoD to place phased arrays on inexpensive platforms such as Unmanned Aerial Vehicles where they have previously proven prohibitively expensive to develop or maintain. ***FY 2018 Plans:*** - Demonstrate arbitrary control of the surface current in a 16 element antenna array. - Continue development of the ACT common module using an advanced 14 nm process node and demonstrate performance improvement compared to the common module developed using a 32 nm node in Phase 1. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The decrease in FY 2019 reflects program completion.	13.000	10.000	-
Title: Adaptive Radio Frequency Technology (ART) ***Description:*** The Adaptive Radio Frequency Technology (ART) program developed a technology base to enable real-time-adaptable radios for individual warfighters and small unmanned systems. ART technologies provided capabilities for next-generation communications, sensing, and electronic warfare, including reconfigurable radios and efficient and compact signal identification capabilities. Goals of the ART program included (1) developing a technology base enabling future radios to survey and adapt to the electromagnetic environment; (2) enabling the rapid deployment of radios in response to changing operational	5.000	-	-

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B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
requirements; and (3) significantly reducing the size, weight, and power (SWaP) of such radios. ART enabled the use of a single design pathway for multiple, unique radio frequency (RF) systems, thus dramatically reducing military procurement and sustainment costs. ART also advanced the hardware and software used in radio frequency (RF) systems by developing a flexible, reconfigurable architecture that can adapt to various RF waveforms.			
Title: Diverse & Accessible Heterogeneous Integration (DAHI) ***Description:*** The Diverse Accessible Heterogeneous Integration (DAHI) program developed the design and manufacturing capabilities required to seamlessly integrate various semiconductors, microelectromechanical systems, photonic (light-manipulating) devices, and thermal management structures into true systems-on-a-chip (SOC). This capability enabled dramatic size, weight, and volume reductions and higher performance for DoD electronic warfare, communications, and radar systems. Historically, chip designers had to decide between the availability, development, and low cost of silicon circuits or the high performance of compound semiconductor (CS) materials. DAHI, however, built on previous DARPA and commercial efforts, which demonstrated that heterogeneously integrating CS and silicon can yield significant performance improvements over silicon or CS alone. DAHI's applied research program focused on developing and demonstrating high-performance SOC for DoD-specific applications. The program also enhanced the manufacturing yield and reliability of heterogeneous integration capabilities and demonstrated innovative, advanced microsystems that leveraged heterogeneous integration. Relevant manufacturing processes were made available to a wide variety of designers from the DoD laboratories, federally funded research and development centers, academia, and industry. This program had advanced technology development efforts funded in PE 0603739E, Project MT-15.	7.000	-	-
Title: Vanishing Programmable Resources (VAPR) ***Description:*** The Vanishing Programmable Resources (VAPR) program created microelectronic and mechanical systems capable of physically vanishing in a controlled, triggerable manner. This advance helped avoid problems associated with unrecovered devices, including their potential use by unauthorized individuals and the compromise of intellectual property. The resulting technologies enabled a range of applications including vanishing sensors for monitoring large areas of the environment and transient airborne vehicles for emergency resupply without requiring pack out of the air delivery vehicle. To support this new class of electronics and mechanical structures, VAPR developed and established an initial set of transient materials and components along with the required manufacturing processes. The resulting systems performed comparably to commercial-off-the-shelf systems while demonstrating system transience that can be programmed, adjusted, triggered, or made to respond to the deployment environment. VAPR technologies were demonstrated through two final test platforms. A vanishing air delivery vehicle capable of precise, gentle drops of small payloads (~3 lbs.) demonstrated the feasibility of transient structural materials. A sensor with a wireless link demonstrated the manufacturability of transient electronics. Both demonstrations were intended to	9.000	-	-

Exhibit R-2A, RDT&E Project Justification: PB 2019 Defense Advanced Research Projects Agency		Date: February 2018
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-01 / *ELECTRONIC TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
fully function on their own and to serve as a leading indicator of the potential systems and concepts-of-operation that VAPR could enable.			
Title: Common Heterogeneous integration & IP reuse Strategies (CHIPS) ***Description:*** The Common Heterogeneous integration & IP reuse Strategies (CHIPS) program aims to develop the design tools and integration standards required to better leverage leading-edge commercial sector technologies in DoD systems. The program aims to realize modular Integrated Circuits (ICs) that integrate designs using different commercial suppliers and silicon technologies. CHIPS will therefore pursue standardized interfaces for integrating a variety of Intellectual Property (IP) blocks in the form of prefabricated chiplets. The chiplets could be reused across applications, manufacturers, and transistor types, allowing DoD to amortize IC design costs across programs, better align electronics design and fabrication with military performance goals, and expand beyond its traditional reliance on the proprietary capabilities of a few on-shore manufacturers. ***FY 2018 Plans:*** - Finalize selection of standards for high-bandwidth interfaces of digital chiplet-based interconnections. - Complete design activities of heterogeneous circuit demonstrations to verify interface standards for chiplet-based integration of digital IP blocks, including commercial and DoD blocks. - Initiate fabrication of heterogeneous circuit demonstrations to verify interface standards for chiplet-based integration of digital IP blocks, including commercial and DoD blocks. - Continue the study of the system level impact of IP re-use for the optimal use of digital functional blocks. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The decrease in FY 2019 reflects the program moving to Project ELT-02.	28.500	28.000	-
Title: Near Zero Energy RF and Sensor Operations (N-ZERO) ***Description:*** The Near Zero Power RF and Sensor Operations (N-ZERO) program will develop and demonstrate the technologies required to extend the lifetimes of remotely-deployed sensors from months to years. Today's state-of-the-art sensors can be pre-placed and remain dormant until awoken by an external trigger or stimulus. However, the active electronics that monitor for external triggers consume power, limiting sensor lifetimes to between weeks and months. N-ZERO seeks to replace these electronics with passive or extremely low-power devices that continuously monitor the environment and wake up active electronics upon detection of a specific trigger. This would eliminate or significantly reduce standby power consumption, ensuring that sensor lifetimes are limited only by the power required to process and communicate confirmed events. In doing so, N-ZERO could enable wireless sensors with drastically increased mission life and help meet DoD's unfulfilled need for a persistent, event-driven sensing capability. N-ZERO's applied research component will focus on developing radio frequency (RF) communications and physical	15.000	20.000	-

Exhibit R-2A, RDT&E Project Justification: PB 2019 Defense Advanced Research Projects Agency		Date: February 2018
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-01 / *ELECTRONIC TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
sensor systems that use energy from an external trigger to collect, process, and detect useful information while rejecting spurious signals and noise. A basic research component is budgeted under PE 0601101E, Project ES-01. ***FY 2018 Plans:*** - Design, fabricate and evaluate microsystems enabling passive or near zero energy collection, processing and detection of RF communications and physical sensor signatures at reduced (100x lower than the original specifications) signal strength. - Identify and engage potential users in the national security space to develop N-ZERO transition opportunities. - Initiate development of a near zero power wake-up circuit designed for a specific DoD application. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The decrease in FY 2019 reflects the program moving to Project ELT-02.			
Title: Circuit Realization At Faster Timescales (CRAFT)	26.000	25.947	-
Description: The Circuit Realization At Faster Timescales (CRAFT) program will develop novel integrated circuit (IC) design flows to reduce by ten times the design and verification effort required for high-performance military electronics. CRAFT will also reduce barriers to the design and fabrication of custom ICs in leading-edge complementary metal oxide semiconductor (CMOS) technology. When selecting electronics for advanced systems, DoD currently must choose between high-performing custom ICs that take years to design and verify or significantly lower-performing general purpose ICs that can be implemented in a few months. The need to protect sensitive IC information further limits DoD's ability to access certain leading-edge commercial electronics. To reduce the design and verification effort, CRAFT will investigate and leverage novel design flows that utilize recent advances in electronic design automation and software design methodologies. These design flows could reduce the manual labor required to develop and verify custom ICs. CRAFT will also explore increased design reuse and flexibility, which will allow DoD to migrate chip fabrication between different foundries or to more advanced technology nodes. Finally, CRAFT will develop and validate various techniques for obscuring sensitive information during the IC manufacturing process, allowing DoD to leverage more of the available onshore semiconductor market. These capabilities can help to ensure that the DoD has multiple potential suppliers for critical ICs and help keep military electronics at the leading edge. ***FY 2018 Plans:*** - Complete initial testing of at least one full object oriented design flow. - Complete third Fin Field Effect Transistor (FinFET) multi-project wafer shuttle run. - Complete FinFET design fabrication on multiple technology nodes at multiple foundries. - Evaluate designs from the second and third multi-project wafer shuttle runs. - Utilize design flow and intellectual property (IP) from the CRAFT repository to complete a DoD reference design.			

Exhibit R-2A, RDT&E Project Justification: PB 2019 Defense Advanced Research Projects Agency		Date: February 2018
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-01 / *ELECTRONIC TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
- Mature new and existing IP obfuscation techniques, evaluate them on DoD-relevant chips, and develop the technologies and techniques required to deploy them for DoD needs. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The decrease in FY 2019 reflects the program moving to Project ELT-02.			
Title: Beyond Scaling - Materials ***Description:*** The Beyond Scaling - Materials program will demonstrate the integration of novel materials into next-generation logic and memory components. Historically, the DoD had taken the lead in shaping the electronics field through research in semiconductor materials, circuits, and processors. However, as DoD focuses on military-specific components and commercial investments eschew the semiconductor space, U.S. fundamental electronics research is stagnant just as an inflection point in Moore's Law (silicon scaling) is about to occur. This program will pursue potential enhancements in electronics that do not rely on Moore's Law, including research not only into new materials but also into the implications of those materials at the device, algorithm, and packaging levels. Research areas will include heterogeneous integration of multiple materials, "sticky logic" devices that combine elements of computation and memory, and leveraging three-dimensional vertical circuit integration to demonstrate dramatic performance improvements with older silicon technologies. The program aims to demonstrate the manufacturability of functioning switches, memory, and novel computational units in a large-scale system. Previous DARPA work on unconventional computing, integration, and reprogrammable memory give confidence in this approach. Basic research for this program is funded within PE 0601101E, Project ES-01. ***FY 2018 Plans:*** - Quantify the value of monolithic vertical integration using leading-edge modern and older technology nodes. - Demonstrate the ability to store the results of computer processing in close proximity to computer logic blocks. - Demonstrate use of unconventional components and designs for non-Von Neumann compute architectures. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The decrease in FY 2019 reflects the program moving to Project ELT-02.	-	19.000	-
Title: Beyond Scaling - Architectures and Designs ***Description:*** The Beyond Scaling - Architectures and Designs program will significantly increase the ease with which DoD can design, deliver, and eventually upgrade critical, customized electronics hardware. As Moore's Law slows and the nation loses the benefit of free, exponential improvements in electronics cost, speed, and power derived from silicon scaling, the DoD will need to maximize the benefits of available silicon technologies by using design tools that enable circuit specialization. This program will develop and demonstrate the tools required for rapidly designing and deploying specialized circuits. Research efforts will explore technologies and techniques such as new domain-specific circuit architectures; co-design of electronics hardware and software;	-	35.000	-

Exhibit R-2A, RDT&E Project Justification: PB 2019 Defense Advanced Research Projects Agency		Date: February 2018
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-01 / *ELECTRONIC TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
tight integration of chip-scale processing blocks and artificial intelligence-enabled processing controllers; and open-source circuit designs. Further research will also develop tools to create exact representations of outdated hardware in the field and to rapidly, cheaply, and safely upgrade these systems with next-generation electronics. Two fundamental goals of this program include (1) reduce the barrier to entry for Complex System on a Chip (SoC) design and (2) manage the utilization of the specialized hardware by enabling the writing of a common code base on top of the customized hardware. Advances under this program will demonstrate a new DoD capability to create specialized hardware and provide benefits by improving electronics systems that do not depend on continued rapid improvements in silicon transistors. Basic research for this program is funded within PE 0601101E, Project ES-01. ***FY 2018 Plans:*** - Demonstrate concepts for machine generation of physical objects that would provide a dramatic reduction in circuit design time. - Demonstrate the ability to construct a system with decomposable pieces that can be rapidly upgraded. - Establish and exhibit the capability to manage specialized accelerators for a variety of codes and applications. - Develop programming language and compiler approaches for dynamic data-dependent optimization of hardware configuration. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The decrease in FY 2019 reflects the program moving to Project ELT-02.			
Accomplishments/Planned Programs Subtotals	190.624	295.447	141.647

C. Other Program Funding Summary ($ in Millions)

N/A

Remarks

D. Acquisition Strategy

N/A

E. Performance Metrics

Specific programmatic performance metrics are listed above in the program accomplishments and plans section.

Exhibit R-2A, RDT&E Project Justification: PB 2019 Defense Advanced Research Projects Agency			Date: February 2018
Appropriation/Budget Activity 0400 / 2	R-1 Program Element (Number/Name) PE 0602716E / *ELECTRONICS TECHNOLOGY*	Project (Number/Name) ELT-02 / *BEYOND SCALING TECHNOLOGY*	

COST ($ in Millions)	Prior Years	FY 2017	FY 2018	FY 2019 Base	FY 2019 OCO	FY 2019 Total	FY 2020	FY 2021	FY 2022	FY 2023	Cost To Complete	Total Cost
ELT-02: *BEYOND SCALING TECHNOLOGY*	-	0.000	0.000	192.200	-	192.200	190.450	191.610	192.400	192.710	-	-

A. Mission Description and Budget Item Justification

The Beyond Scaling Technology project recognizes that phenomenal advancements in electronics will face the fundamental limits of silicon technology in the early 21st century, presenting a barrier that must be overcome in order for progress to continue. This project will therefore pursue potential electronics performance advancements that do not rely on Moore's Law but instead leverage circuit specialization, to include leveraging materials, architectures, and designs that are designed to suit a specific need. Programs within the Beyond Scaling project will look at reducing barriers to making specialized circuits in today's silicon hardware. They will also explore alternatives to traditional circuit architectures, for instance by exploiting chip-scale heterogeneous integration of differing material technologies, using "sticky logic" devices that combine computation and memory functions, and vertical circuit integration to optimize electronic devices. This Project is not a new start. It aggregates and continues Beyond Scaling programs that were initiated in PEs/Projects 0602716E/ELT-01 and 0602303E/IT-02 and IT-03.

B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
Title: Beyond Scaling - Materials	-	-	33.254
Description: The Beyond Scaling - Materials program will demonstrate the integration of novel materials into next-generation logic and memory components. Historically, the DoD had taken the lead in shaping the electronics field through research in semiconductor materials, circuits, and processors. However, as DoD focuses on military-specific components and commercial investments eschew the semiconductor space, U.S. fundamental electronics research is stagnant just as an inflection point in Moore's Law (silicon scaling) is about to occur. This program will pursue potential enhancements in electronics that do not rely on Moore's Law, including research not only into new materials but also into the implications of those materials at the device, algorithm, and packaging levels. Research areas will include heterogeneous integration of multiple materials, "sticky logic" devices that combine elements of computation and memory, and leveraging three-dimensional vertical circuit integration to demonstrate dramatic performance improvements with older silicon technologies. The program aims to demonstrate the manufacturability of functioning switches, memory, and novel computational units in a large-scale system. Previous DARPA work on unconventional computing, integration, and reprogrammable memory give confidence in this approach. Basic research for this program is funded within PE 0601101E, Project ES-02.			
FY 2019 Plans: - Complete design and initiate fabrication of a significant computation block based on vertically integrated monolithic logic and memory components. - Demonstrate that leading-edge System on a Chip (SoC) performance can be achieved using an older technology node through the use of monolithic vertical integration.			

Exhibit R-2A, RDT&E Project Justification: PB 2019 Defense Advanced Research Projects Agency		Date: February 2018
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
- Validate the performance benefits of novel and unconventional circuit topologies which utilize the peculiar physics of unique materials and components not used in traditional silicon processing. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The increase in FY 2019 reflects the program moving from Project ELT-01.			
Title: Beyond Scaling - Architectures and Designs ***Description:*** The Beyond Scaling - Architectures and Designs program will significantly increase the ease with which DoD can design, deliver, and eventually upgrade critical, customized electronics hardware. As Moore's Law slows and the nation loses the benefit of free, exponential improvements in electronics cost, speed, and power derived from silicon scaling, the DoD will need to maximize the benefits of available silicon technologies by using design tools that enable circuit specialization. This program will develop and demonstrate the tools required for rapidly designing and deploying specialized circuits. Research efforts will explore technologies and techniques such as new domain-specific circuit architectures; co-design of electronics hardware and software; tight integration of chip-scale processing blocks and artificial intelligence-enabled processing controllers; and open-source circuit designs. Further research will also develop tools to create exact representations of outdated hardware in the field and to rapidly, cheaply, and safely upgrade these systems with next-generation electronics. Two fundamental goals of this program include (1) reduce the barrier to entry for Complex System on a Chip (SoC) design and (2) manage the utilization of the specialized hardware by enabling the writing of a common code base on top of the customized hardware. Advances under this program will demonstrate a new DoD capability to create specialized hardware and provide benefits by improving electronics systems that do not depend on continued rapid improvements in silicon transistors. Basic research for this program is funded within PE 0601101E, Project ES-02. ***FY 2019 Plans:*** - Create software which allows for reduction in design time of 10x for a given design applied to both a chip design and a board design. - Demonstrate that a hardware scheduler will allow for the optimal routing on a specialized integrated circuit in situ of operation. - Design system-on-chips (SOCs) with heterogeneous mix of processors and algorithm accelerators to solve domain-specific compute problems with good power and performance. - Implement an intelligent scheduler to utilize the mix of heterogeneous processors and demonstrate the scheduler on commercially available SOCs. - Demonstrate pathways to apply machine learning to physical design and creation of annotated datasets for machine learning. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The increase in FY 2019 reflects the program moving from Project ELT-01.	-	-	67.786
Title: Common Heterogeneous integration & IP reuse Strategies (CHIPS)	-	-	15.500

Exhibit R-2A, RDT&E Project Justification: PB 2019 Defense Advanced Research Projects Agency		Date: February 2018
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
Description: The Common Heterogeneous integration & IP reuse Strategies (CHIPS) program aims to develop the design tools and integration standards required to better leverage leading-edge commercial sector technologies in DoD systems. The program aims to realize modular Integrated Circuits (ICs) that integrate designs using different commercial suppliers and silicon technologies. CHIPS will therefore pursue standardized interfaces for integrating a variety of Intellectual Property (IP) blocks in the form of prefabricated chiplets. The chiplets could be reused across applications, manufacturers, and transistor types, allowing DoD to amortize IC design costs across programs, better align electronics design and fabrication with military performance goals, and expand beyond its traditional reliance on the proprietary capabilities of a few on-shore manufacturers. ***FY 2019 Plans:*** - Complete module design activities to determine performance and program benefits of new processes enabled by the program. - Initiate fabrication of approved modules to determine performance and program benefits of new processes enabled by the program. - Continue the study of the system level impact of IP re-use for the optimal use of digital and analog functional blocks. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The increase in FY 2019 reflects the program moving from Project ELT-01.			
Title: System Security Integrated Through Hardware and firmware (SSITH)	-	-	22.790
Description: The System Security Integrated Through Hardware and firmware (SSITH) program seeks to secure DoD and commercial electronic systems against cybersecurity threats by developing novel hardware/firmware security architectures and hardware design methodologies. Current responses to cybersecurity attacks typically consist of developing and deploying software patches to address specific vulnerabilities in a software firewall without addressing potential vulnerabilities in the underlying hardware architecture. To address this challenge, SSITH will drive new research in electronics hardware security and exploit current research in areas such as cryptographic-based computing and hardware verification. Implementation of these advanced ideas has been enabled by the extremely capable semiconductor technology driven by Moore's Law. The program will also investigate flexible hardware architectures that adapt to and limit the impact of new cybersecurity attacks. Finally, SSITH will seek to mitigate the potential negative impact of new security protection architectures on system performance and power usage. Once developed, SSITH capabilities will be applicable to both commercial and military electronic systems. ***FY 2019 Plans:*** - Implement new hardware architectures on the Field-Programmable Gate Array (FPGA) demonstration platforms that demonstrate scalable, flexible, and robust protection against external attacks on hardware. - Utilize simulation and hardware emulation to confirm the expected improvement in protection of the new hardware architectures relative to current software only protection.			

Exhibit R-2A, RDT&E Project Justification: PB 2019 Defense Advanced Research Projects Agency		Date: February 2018
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
- Evaluate SSITH security approaches through independent Red Team attack on the security architectures as implemented on platform FPGA hardware. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The increase in FY 2019 reflects the program moving from PE 0602303E, Project IT-03.			
Title: Hierarchical Identify Verify Exploit (HIVE) ***Description:*** The Hierarchical Identify Verify Exploit (HIVE) program will pursue new hardware architectures and algorithms for rapidly integrating information from a variety of sources, increasing battlefield situational awareness. To develop operationally significant intelligence, human analysts today watch live battlefield feeds to detect items of interest, fusing together and interpreting information from multiple sensors and sources. The amount of information gathered, however, is quickly outstripping the human ability to review, process, fuse, and interpret. To resolve this challenge, HIVE seeks to leverage improvements in machine learning and artificial intelligence to augment the analyst's ability to integrate large streams of data. The program will investigate advances in chip architecture and data analytics algorithms that can allow machines to infer meaning out of data based on the information needs of the warfighter. Program success would therefore enable the warfighter to understand far more of the battlefield in real time. ***FY 2019 Plans:*** - Improve the toolsets based on information gathered from previous testing and deliver a beta version of the software. - Finalize the chip design and deliver the final design to the chip fabrication facility. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The increase in FY 2019 reflects the program moving from PE 0602303E, Project IT-02.	-	-	17.600
Title: Circuit Realization At Faster Timescales (CRAFT) ***Description:*** The Circuit Realization At Faster Timescales (CRAFT) program will develop novel integrated circuit (IC) design flows to reduce by ten times the design and verification effort required for high-performance military electronics. CRAFT will also reduce barriers to the design and fabrication of custom ICs in leading-edge complementary metal oxide semiconductor (CMOS) technology. When selecting electronics for advanced systems, DoD currently must choose between high-performing custom ICs that take years to design and verify or significantly lower-performing general purpose ICs that can be implemented in a few months. The need to protect sensitive IC information further limits DoD's ability to access certain leading-edge commercial electronics. To reduce the design and verification effort, CRAFT will investigate and leverage novel design flows that utilize recent advances in electronic design automation and software design methodologies. These design flows could reduce the manual labor required to develop and verify custom ICs. CRAFT will also explore increased design reuse and flexibility, which will allow DoD to migrate chip fabrication between different foundries or to more advanced technology nodes. Finally, CRAFT will develop and	-	-	7.000

Exhibit R-2A, RDT&E Project Justification: PB 2019 Defense Advanced Research Projects Agency		Date: February 2018
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
validate various techniques for obscuring sensitive information during the IC manufacturing process, allowing DoD to leverage more of the available onshore semiconductor market. These capabilities can help to ensure that the DoD has multiple potential suppliers for critical ICs and help keep military electronics at the leading edge. ***FY 2019 Plans:*** - Complete the fourth multi-project wafer shuttle run with the final CRAFT design flow. - Finalize the IP repository design and setup to allow access to a design flow and related IP for DoD use. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The increase in FY 2019 reflects the program moving from Project ELT-01.			
Title: Near Zero Energy RF and Sensor Operations (N-ZERO) ***Description:*** The Near Zero Power RF and Sensor Operations (N-ZERO) program will develop and demonstrate the technologies required to extend the lifetimes of remotely-deployed sensors from months to years. Today's state-of-the-art sensors can be pre-placed and remain dormant until awoken by an external trigger or stimulus. However, the active electronics that monitor for external triggers consume power, limiting sensor lifetimes to between weeks and months. N-ZERO seeks to replace these electronics with passive or extremely low-power devices that continuously monitor the environment and wake up active electronics upon detection of a specific trigger. This would eliminate or significantly reduce standby power consumption, ensuring that sensor lifetimes are limited only by the power required to process and communicate confirmed events. In doing so, N-ZERO could enable wireless sensors with drastically increased mission life and help meet DoD's unfulfilled need for a persistent, event-driven sensing capability. N-ZERO's applied research component will focus on developing radio frequency (RF) communications and physical sensor systems that use energy from an external trigger to collect, process, and detect useful information while rejecting spurious signals and noise. A basic research component is budgeted under PE 0601101E, Project ES-01. ***FY 2019 Plans:*** - Design, implement and test signal processing to improve the detection and classification capabilities of N-ZERO sensor systems in the presence of significant background interference. - Facilitate transition opportunities for microsystems enabling passive or near zero energy collection, processing and detection of RF communications and physical sensor signatures at reduced (100x lower than the original specifications) signal strength. - Continue the development of a near zero power wake-up circuit designed for a specific DoD application. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The increase in FY 2019 reflects the program moving from Project ELT-01.	-	-	11.079
Title: Ensured Communication Link for Identification Friend or Foe (ECLIFF)	-	-	9.191

Exhibit R-2A, RDT&E Project Justification: PB 2019 Defense Advanced Research Projects Agency		Date: February 2018
Appropriation/Budget Activity 0400 / 2	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	**Project (Number/Name)** ELT-02 / *BEYOND SCALING TECHNOLOGY*

B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
Description: The Ensured Communication Link for Identification Friend or Foe (ECLIFF) program aims to provide communication links for Identification Friend or Foe (IFF) capabilities with a reduced radio frequency (RF) signature, improved performance against jamming and interference, and a compact form factor. ECLIFF will address the challenge of identifying friendly assets and personnel in congested electromagnetic environments and in environments where there is a strong penalty for stray radio emissions. The current IFF system operates with a limited instantaneous RF bandwidth (IBW), which makes hiding signals from adversaries difficult and leaves the system vulnerable to jamming and interference. ECLIFF will explore alternative technologies to enable ~25 times greater IBW. These technologies should also enable IFF systems to use alternate channels at higher frequency bands. The resulting ECLIFF system could employ DARPA-developed technologies such as high-speed data converters, heterogeneous integration, and envelope-tracking transmitter technology. The novel combination of these technologies in the final ECLIFF system will be critical for dramatic size, weight, power, and cost reduction and performance improvements. The miniaturization realized with the ECLIFF platform should make the capability useful for both large platforms and portable applications such as unmanned air vehicle, man-portable, and even hand-held devices. The ECLIFF program will culminate with a demonstration of the technology in a relevant environment, lowering the risk for transition to a fielded system. ***FY 2019 Plans:*** - Complete system trade study for IFF solution. - Begin initial design of integrated circuit hardware to implement ECLIFF solution. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The increase in FY 2019 reflects program initiation.			
Title: Digital RF Battlespace Emulator (DRBE) ***Description:*** The Digital RF Battlespace Emulator (DRBE) program aims to develop a large-scale, interactive, emulated radiofrequency (RF) environment, providing DoD with the much needed capability to cost-effectively evaluate adaptive, intelligent, and spatially distributed next-generation RF systems. Current U.S. test infrastructure is no longer able to successfully exercise RF systems in relevant environments, which should account for hundreds of DoD systems coordinating against hundreds of adversary systems. Due to the critical dependency of nearly all platforms and missions on the RF spectrum and the increasingly advanced RF capabilities of peer adversaries, current infrastructure limitations represent a critical capability gap. Existing test approaches are either: 1) small-scale laboratory tests under well controlled but unrealistic conditions or 2) massive training exercises, which occur at most annually due to the required cost and manpower and do not fully collect necessary data. To overcome these limitations, DRBE will leverage advances in massively multi-core computing hardware and high-bandwidth digital cross connects to emulate realistic RF environments that account for RF platform movement, signal propagation effects and delays, signal interference, and interactions between RF systems. DRBE will pursue three technical thrust areas: architecture, massively multi-core computing, and scenario modeling. The resulting test environment should allow plug-and-play connections	-	-	8.000

Exhibit R-2A, RDT&E Project Justification: PB 2019 Defense Advanced Research Projects Agency		Date: February 2018
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B. Accomplishments/Planned Programs ($ in Millions)	FY 2017	FY 2018	FY 2019
for hundreds of RF systems in a 100 km battlespace test. Multi-system exercises could then be quickly executed through many different combat scenarios and variations, with RF systems employing war reserve modes forbidden during open-air testing. DRBE should therefore serve to develop CONOPS, inform battle plans, and fine-tune the performance of both individual and large groups of RF systems. ***FY 2019 Plans:*** - Conduct architecture scaling analysis to define a solution supporting hundreds of RF systems. - Demonstrate basic physical building blocks that will be able to handle the immense throughput expected. ***FY 2018 to FY 2019 Increase/Decrease Statement:*** The increase in FY 2019 reflects program initiation.			
Accomplishments/Planned Programs Subtotals	-	-	192.200

C. Other Program Funding Summary ($ in Millions)

N/A

Remarks

D. Acquisition Strategy

N/A

E. Performance Metrics

Specific programmatic performance metrics are listed above in the program accomplishments and plans section.