Exhibit R-2, RDT&E Budget Item Justification: PB 2016 Defense Advanced Research Projects Agency	**Date:** February 2015
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*

COST ($ in Millions)	Prior Years	FY 2014	FY 2015	FY 2016 Base	FY 2016 OCO	FY 2016 Total	FY 2017	FY 2018	FY 2019	FY 2020	Cost To Complete	Total Cost
Total Program Element	-	222.287	169.203	174.798	-	174.798	170.783	198.083	195.175	198.347	-	-
ELT-01: *ELECTRONICS TECHNOLOGY*	-	222.287	169.203	174.798	-	174.798	170.783	198.083	195.175	198.347	-	-

A. Mission Description and Budget Item Justification

This program element is budgeted in the Applied Research budget activity because its objective is to develop electronics that make a wide range of military applications possible.

Advances in microelectronic device technologies, including digital, analog, photonic and MicroElectroMechanical Systems (MEMS) devices, continue to have significant impact in support of defense technologies for improved weapons effectiveness, improved intelligence capabilities and enhanced information superiority. The Electronics Technology program element supports the continued advancement of these technologies through the development of performance driven advanced capabilities, exceeding that available through commercial sources, in electronic, optoelectronic and MEMS devices, semiconductor device design and fabrication techniques, and new materials and material structures for device applications. A particular focus for this work is the exploitation of chip-scale heterogeneous integration technologies that permit the optimization of device and integrated module performance.

The phenomenal progress in current electronics and computer chips will face the fundamental limits of silicon technology in the early 21st century, a barrier that must be overcome in order for progress to continue. Another thrust of the program element will explore alternatives to silicon-based electronics in the areas of new electronic devices, new architectures to use them, new software to program the systems, and new methods to fabricate the chips. Approaches include nanotechnology, nanoelectronics, molecular electronics, spin-based electronics, quantum-computing, new circuit architectures optimizing these new devices, and new computer and electronic systems architectures. Projects will investigate the feasibility, design, and development of powerful information technology devices and systems using approaches for electronic device designs that extend beyond traditional Complementary Metal Oxide Semiconductor (CMOS) scaling, including non-silicon-based materials technologies to achieve low cost, reliable, fast and secure computing, communication, and storage systems. This investigation is aimed at developing new capabilities from promising directions in the design of information processing components using both inorganic and organic substrates, designs of components and systems leveraging quantum effects and chaos, and innovative approaches to computing designs incorporating these components for such applications as low cost seamless pervasive computing, ultra-fast computing, and sensing and actuation devices.

This project has five major thrusts: Electronics, Photonics, MicroElectroMechanical Systems, Architectures, Algorithms, and other Electronic Technology research.

Exhibit R-2, RDT&E Budget Item Justification: PB 2016 Defense Advanced Research Projects Agency	**Date:** February 2015
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*

B. Program Change Summary ($ in Millions)

	FY 2014	FY 2015	FY 2016 Base	FY 2016 OCO	FY 2016 Total
Previous President's Budget	233.469	179.203	183.439	-	183.439
Current President's Budget	222.287	169.203	174.798	-	174.798
Total Adjustments	-11.182	-10.000	-8.641	-	-8.641
• Congressional General Reductions	-	-			
• Congressional Directed Reductions	-	-10.000			
• Congressional Rescissions	-	-			
• Congressional Adds	-	-			
• Congressional Directed Transfers	-	-			
• Reprogrammings	-4.280	-			
• SBIR/STTR Transfer	-6.902	-			
• TotalOtherAdjustments	-	-	-8.641	-	-8.641

Change Summary Explanation

FY 2014: Decrease reflects reprogrammings and the SBIR/STTR transfer.
FY 2015: Decrease reflects congressional reduction.
FY 2016: Decrease reflects completion of several electronics technology programs such as: Nitride Electronic NeXt-Generation Technology, Microscale Plasma Devices, and Micro-coolers for Focal Plane Arrays.

C. Accomplishments/Planned Programs ($ in Millions)	**FY 2014**	**FY 2015**	**FY 2016**
Title: Adaptive Radio Frequency Technology (ART)	29.009	24.003	15.550
Description: There is a critical ongoing military need for flexible, affordable, and small size, weight and power (SWaP) real-time-adaptable military electromagnetic interfaces. The Adaptive Radio Frequency Technology (ART) program will provide the warfighter with a new, fully adaptive radio platform capable of sensing the electromagnetic and waveform environment in which it operates, making decisions on how to best communicate in that environment, and rapidly adapting its hardware to meet ever-changing requirements, while simultaneously significantly reducing the SWaP of such radio nodes. ART technology will also provide each warfighter, as well as small-scale unmanned platforms, with compact and efficient signal identification capabilities for next-generation cognitive communications, and sensing and electronic warfare applications. ART technology will also enable rapid radio platform deployment for new waveforms and changing operational requirements. The project will remove the separate design tasks needed for each unique Radio Frequency (RF) system, which will dramatically reduce the procurement and sustainment cost of military systems. ART aggregates the Feedback Linearized Microwave Amplifiers program, the Analog Spectral Processing program, and Chip Scale Spectrum Analyzers (CSSA) program, and initiates new thrusts in Cognitive Low-energy Signal Analysis and Sensing Integrated Circuits (CLASIC), and Radio-Frequency Field-Programmable Gate Arrays (RF-FPGA).			

C. Accomplishments/Planned Programs ($ in Millions)	FY 2014	FY 2015	FY 2016
FY 2014 Accomplishments: - Demonstrated reconfigurable RF circuit (RF-FPGA) technologies at the component and system levels along with the necessary computer-aided design approaches. - Demonstrated 100x improvement in the number of times high performance phase-change switches can be switched on and off. - Developed and demonstrated new integration process for phase-change switches that will enable demonstration at multi-system reconfiguration level. - Manufactured a second-generation single reconfigurable integrated circuit optimized for different applications such as comms, signals intelligence (SIGINT), and wideband Electronic Warfare (EW) with access up to 2250 RF states. This chip serves as a prototype for how ART technology can lead the way to life-cycle cost reduction. - Demonstrated advanced concepts for signal recognition at the hardware level and initiate plans for transitioning these approaches to relevant DoD systems. - Demonstrated applicability of tunable filters for dynamic frequency allocation in a fielded radio system. ***FY 2015 Plans:*** - Demonstrate final circuit design technologies including microwave switches, frequency synthesis, and RF functionality. - Demonstrate a fully reconfigurable RF filter element with serial addressing of the components in an appropriate package form factor. - Optimize the RF phase-change switch technology with concentration on reliability along with performing a final RF-FPGA demonstration. - Demonstrate computer aided software flow with advanced fully reconfigurable RF circuit technology at the hardware system level. - Begin integration of a reconfigurable RF front-end system with a reconfigurable, digital back-end system to demonstrate end-to-end reconfigurability after the aperture. ***FY 2016 Plans:*** - Investigate transition plans for a fully reconfigurable RF circuit technology at the component and system levels. - Continue integration of a reconfigurable RF front-end system with a reconfigurable, digital back-end system to demonstrate end-to-end reconfigurability after the aperture.			
Title: Diverse & Accessible Heterogeneous Integration (DAHI) ***Description:*** Prior DARPA efforts have demonstrated the ability to monolithically integrate different semiconductor types to achieve near-ideal "mix-and-match" capability for DoD circuit designers. Specifically, the Compound Semiconductor Materials On Silicon (COSMOS) program enabled transistors of Indium Phosphide (InP) to be freely mixed with silicon complementary metal-oxide semiconductor (CMOS) circuits to obtain the benefits of both technologies (very high speed and very high circuit complexity/density, respectively). The Diverse & Accessible Heterogeneous Integration (DAHI) effort will take this capability to the next	31.663	29.400	15.983

Exhibit R-2, RDT&E Budget Item Justification: PB 2016 Defense Advanced Research Projects Agency		**Date:** February 2015
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	

C. Accomplishments/Planned Programs ($ in Millions)	**FY 2014**	**FY 2015**	**FY 2016**

level, ultimately offering the seamless co-integration of a variety of semiconductor devices (for example, Gallium Nitride, Indium Phosphide, Gallium Arsenide, Antimonide Based Compound Semiconductors), microelectromechanical (MEMS) sensors and actuators, photonic devices (e.g., lasers, photo-detectors) and thermal management structures. This capability will revolutionize our ability to build true "systems on a chip" (SoCs) and allow dramatic size, weight and volume reductions for a wide array of system applications.

In the Applied Research part of this program, high performance RF/optoelectronic/mixed-signal systems-on-a-chip (SoC) for specific DoD transition applications will be developed as a demonstration of the DAHI technology. To provide maximum benefit to the DoD, these processes will be transferred to a manufacturing flow and made available (with appropriate computer aided design support) to a wide variety of DoD laboratory, Federally Funded Research and Development Center (FFRDC), academic and industrial designers. Manufacturing yield and reliability of the DAHI technologies will be characterized and enhanced. This program has basic research efforts funded in PE 0601101E, Project ES-01, and advanced technology development efforts funded in PE 0603739E, Project MT-15.

FY 2014 Accomplishments:
- Continued to develop new CMOS-compatible processes to achieve heterogeneous integration with diverse types of compound semiconductor transistors, MEMS, and non-silicon photonic devices, including interconnect and thermal management approaches.
- Developed three-technology wafer-bonding-based processes for heterogeneous integration, and processes for heterogeneous integration of InP and GaN transistors, Gallium nitride (GaN) MEMS devices, magnetic materials, and microfluidic thermal management structures on silicon and silicon carbide substrates.
- Continued manufacturing, yield and reliability enhancement for multi-user foundry capability based on developed diverse heterogeneous integration processes.
- Continued design and fabrication of high complexity heterogeneously integrated RF/optoelectronic/mixed signal and circuits, such as wide band RF transmitters, advanced mixed signal integrated systems, optoelectronic RF signal sources, and laser-radar systems.
- Completed circuit designs for initial heterogeneous integration multi-project wafer foundry fabrication run, which are currently being fabricated.

FY 2015 Plans:
- Complete development of new CMOS-compatible processes to achieve heterogeneous integration with diverse types of compound semiconductor transistors, MEMS, and non-silicon photonic devices, including interconnect and thermal management approaches.

C. Accomplishments/Planned Programs ($ in Millions)	FY 2014	FY 2015	FY 2016
- Complete manufacturing, yield and reliability enhancement for multi-user foundry capability based on developed diverse heterogeneous integration processes. - Complete design and fabrication of high complexity heterogeneously integrated RF/optoelectronic/mixed signal and circuits, such as wide band RF transmitters, advanced mixed signal integrated systems, optoelectronic RF signal sources, and laser radar systems. ***FY 2016 Plans:*** - Demonstrate heterogeneous integration of advanced node Silicon CMOS processes achieved with diverse types of compound semiconductor transistors, MEMS, and non-silicon photonic devices, including interconnect and thermal management approaches. - Transition multi-user foundry interface to independent design service from proprietary foundry model to enable community access to diverse heterogeneous integration processes.			
Title: IntraChip Enhanced Cooling (ICECool) ***Description:*** The IntraChip Enhanced Cooling (ICECool) program is exploring disruptive technologies that will remove thermal barriers to the operation of military electronic systems, while significantly reducing size, weight, and power consumption. These thermal barriers will be removed by integrating thermal management into the chip, substrate, or package technology. Successful completion of this program will raise chip heat removal rates to above 1 kilowatt/cm^2 and chip package heat removal density to above 1kilowatt/cm^3 in RF arrays and embedded computers. Specific areas of focus in this program include overcoming limiting evaporative and diffusive thermal transport mechanisms at the micro/nano scale to provide an order-of-magnitude increase in on-chip heat flux and heat removal density, determining the feasibility of exploiting these mechanisms for intrachip thermal management, characterizing the performance limits and physics-of-failure of high heat density, intrachip cooling technologies, and integrating chip-level thermal management techniques into prototype high power electronics in RF arrays and embedded computing systems. ***FY 2014 Accomplishments:*** - Prepared and refined initial thermal models of intrachip cooling to explain and predict experimental results. - Demonstrated proof of concept of fundamental building blocks of evaporative intrachip/interchip thermal management including microfabrication in relevant electronic substrates and preliminary thermofluid results. - Designed thermal test vehicles in the form factor of high power amplifiers (HPAs) and high performance computers (HPCs) and demonstrated that embedded microfluidic cooling had the potential to manage heat fluxes of 1 kW/cm^2 and densities of 1 kW/cm^3 through modeling and proof of concept experiments. ***FY 2015 Plans:***	19.500	18.000	17.000

C. Accomplishments/Planned Programs ($ in Millions)	FY 2014	FY 2015	FY 2016
- Demonstrate the full implementation of the fundamental building blocks of evaporative intrachip/interchip cooling including embedded micron-scale microfluidic channels in Silicon (Si), Silicon Carbide (SiC), and diamond; two-phase flow approaching 95% vapor exit quality, and integrated thin-film thermoelectric devices. - Demonstrate HPAs and embedded HPCs thermal test vehicles that can successfully handle heat fluxes of 1 kW/cm^2, hot spots of 30 kW/cm2 (HPAs) or 2 kW/cm^2 (HPCs), and reduce the thermal resistance of the test vehicle by 3x compared to the State of the Art (SOA) baseline. - Design application-oriented electrical test vehicles to demonstrate the performance benefits of embedded microfluidic cooling and relate these results to system-level performance and size, weight, power and cost (SWaPC) through the use of intrachip thermal management technologies. - Design fully-functional HPAs and HPCs to demonstrate the thermal and electrical performance benefits of embedded microfluidic cooling where the 3x or greater reduction in thermal resistance with enable a 3x or greater increase in output power (HPAs) or computational performance (HPCs) compared to the State of the Art (SOA) baseline. ***FY 2016 Plans:*** - Perform reliability testing of ICECool electrical demonstration modules to prove out mean time to failure and compatibility with relevant Military specifications. - Engage in transition activities for the ICECool technology to include insertion of ICECool enabled components in relevant subsystems such as transmit/receive modules and embedded airborne computing platforms.			
Title: In vivo Nanoplatforms (IVN) ***Description:*** The In vivo Nanoplatforms (IVN) program seeks to develop the nanoscale systems necessary for in vivo sensing and physiologic monitoring and delivery vehicles for targeted biological therapeutics against chemical and biological (chem-bio) threat agents. The nanoscale components to be developed will enable continuous in vivo monitoring of both small (e.g., glucose, nucleic acids, biomarkers) and large molecules (e.g., biological threat agents). A reprogrammable therapeutic platform that targets gene regulatory sequences will enable tailored therapeutic delivery to specific areas of the body (e.g., cells, tissue, compartments) in response to traditional, emergent, and engineered threats. The key challenges to developing these systems include safety, toxicity, biocompatibility, sensitivity, response, and targeted delivery. The IVN program will have diagnostic and therapeutic goals that enable a versatile, rapidly adaptable system to provide operational support to the warfighter in any location. ***FY 2014 Accomplishments:*** - Achieved a safe in vivo nanoplatform sensor to detect military-relevant analytes (e.g., nucleic acids) in an animal model with a robust signal for at least six months. - Achieved a safe and effective in vivo nanoplatform therapeutic to reduce a military-relevant pathogen in a small animal model.	23.388	14.500	9.765

C. Accomplishments/Planned Programs ($ in Millions)	FY 2014	FY 2015	FY 2016
- Updated regulatory approval pathway of identified safe and effective diagnostic and therapeutic nanoplatforms. ***FY 2015 Plans:*** - Demonstrate broad capability of in vivo nanoplatform sensors to detect additional military-relevant analytes (e.g., pH, cortisol) in an animal model with a robust signal. - Demonstrate broad capability of in vivo nanoplatform therapeutics targeting gene regulatory sequences to maintain force health and reduce additional military-relevant pathogens or disease cofactors (e.g., multi-drug resistant bacteria, neurological disease) in an animal model. - Update regulatory approval pathway with results from animal model safety and efficacy testing. ***FY 2016 Plans:*** - Demonstrate enhanced therapeutic performance via molecular targeting approaches in an animal model. - Demonstrate the ability of skin-based sensors to detect physiologically relevant molecules (e.g., pH, cortisol) in an animal model. - Demonstrate the ability of an in vivo nanoplatform to protect against infectious disease in an animal model. - Continue to update regulatory approval pathway with results from animal model safety and efficacy testing.			
Title: Pixel Network (PIXNET) for Dynamic Visualization ***Description:*** The PIXNET program addresses the squad level capability gap for target detection, recognition and identification in all-weather and day/night missions through real-time fusion of visible and thermal infrared (IR) imagery. The vision of the program is to offer the warfighter a small and versatile camera that would be affordable for individual soldiers and provide multiple band imagery with fusion capability to take full advantage of different wavelength-band phenomenology in a compact single unit. In the future, the availability of the PIXNET camera would enable a peer-to-peer networked system for image sharing within a squad, thereby providing a better common operating picture of the battlefield and significantly enhancing the warfighter's situational understanding. The program aims to develop a low size, weight and power (SWaP), low cost, soldier-portable multiband infrared camera that will provide real-time single and multiple band imagery using thermal and reflected-illumination bands. The camera will also provide fused reflective and thermal band imagery on demand. The use of fused imagery in the PIXNET design will allow the soldier to detect camouflaged targets and distinguish targets from decoys. The PIXNET camera will eliminate limitations posed by current capability, allowing detection, recognition and identification of targets from a single camera whether in daylight or no-light conditions. The PIXNET program will focus on a significant reduction in SWaP and cost of infrared sensor components to enable portability and ability to deploy widely to all participants in the theater. The emphasis on a small form will naturally enable new opportunities such as surveillance with small Unmanned Aerial Vehicles (UAV), rifle sights with multiple bands, and vehicle-mounted, helmet-mounted and handheld surveillance systems. The phenomenology of different infrared wavelengths will be exploited. The	23.700	13.000	10.250

Exhibit R-2, RDT&E Budget Item Justification: PB 2016 Defense Advanced Research Projects Agency	Date: February 2015
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*

C. Accomplishments/Planned Programs ($ in Millions)	FY 2014	FY 2015	FY 2016
combination of a smart phone and PIXNET camera at the soldier level will enable more effective tactics, techniques and procedures (TTP) over the current capability. The PIXNET program takes advantage of the computing capability of smart phones to process and fuse multicolor images and send them as videos or still images to the warfighter's helmet-mounted display via a wireless or wired connection. ***FY 2014 Accomplishments:*** - Developed and reviewed IR camera design and overall architecture that will demonstrate digital image data transmission and signal processing via wireless connectivity using an android based platform. - Identified parameters required for multicolor helmet-mounted technology for very low SWaP multi-color IR camera. - Completed short wave (SW)/mid-wave (MW) optics design for clip-on weapon sight. - Identified wireless interface protocols for rifles/weapons and helmet displays that are compliant with dismount requirements. - Performed final design of the long-wave IR/very-near IR (LWIR/VNIR) camera cores, optic lens assemblies, display module, image fusion network power components, helmet package, image processing pipeline, and embedded software applications. ***FY 2015 Plans:*** - Demonstrate brass board components for the LWIR/VNIR helmet camera. - Refine algorithms to fuse data from thermal and reflective bands with good image registration. - Complete interim small form-factor camera integration and demonstrate connectivity to heads-up display and Android-based platform. - Complete Readout Integrated Circuit (ROIC) tapeout and SW/MW fabrication. - Complete fabrication of LWIR/VNIR and start final integration of helmet camera. - Demonstrate multicolor image acquisition by interim PIXNET camera, data transmission to Android platform, image fusion by Android platform, and viewing of fused imagery on heads-up display. - Evaluate and refine the multicolor PIXNET camera based on Phase 1 brass-board demonstration. - Update the fusion and rendering algorithms to meet the system requirements. ***FY 2016 Plans:*** - Implement algorithms into final camera and laptop to demonstrate functionality. - Package and integrate multicolor systems into final form factor. - Demonstrate helmet mounted and clip-on weapon sight video on Smart Phone with final camera deliverables.			
Title: Arrays at Commercial Timescales (ACT) ***Description:*** Phased arrays are critical system components for high performance military electronics with widespread applications in communications, electronic warfare and radar. The DoD relies heavily on phased arrays to maintain technological superiority in nearly every theater of conflict. The DoD cannot update these high cost specialized arrays at the pace necessary to effectively	23.856	25.000	26.550

Exhibit R-2, RDT&E Budget Item Justification: PB 2016 Defense Advanced Research Projects Agency	Date: February 2015
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	R-1 Program Element (Number/Name) PE 0602716E / *ELECTRONICS TECHNOLOGY*

C. Accomplishments/Planned Programs ($ in Millions)	FY 2014	FY 2015	FY 2016
counter adversarial threats under development using commercial-of-the-shelf components that can undergo technology refresh far more frequently. The Arrays at Commercial Timescales (ACT) program will develop adaptive and standardized digital-at-every-element arrays. The hand designed, static analog beamformers will be replaced with cost effective digital array systems capable of a yearly technology refresh. By doing so, phased arrays will become ubiquitous throughout the DoD, moving onto many platforms for which phased arrays had been previously prohibitively expensive to develop or maintain. The basic research component of this program is budgeted under PE 0601101E, Project ES-01. ***FY 2014 Accomplishments:*** - Initiated development of common hardware components for phased-array elements that can be seamlessly integrated into a wide range of platforms and implemented the first iteration of the common components in a state-of-the-art fabrication process. - Initiated the development of digital array systems with performance capabilities that evolve with Moore's law at commercial time scales. - Performed initial characterization of common module data converter components demonstrating high RF sample rates of 64 Giga samples per second. - Demonstrated that non-linear equalization can extend the signal dynamic range by more than 20 decibels. - Initiated the development of electromagnetic (EM) interface elements capable of reconfiguring for various array use cases and operational specifications. - Demonstrated reconfigurability of EM interface components for various array performance specifications and demonstrated compatibility with common digital back-end. - Demonstrated optical actuation of Germanium Telluride phase change switches for reconfigurable antennas with a high on/off ratio of 10,000:1. - Identified government application spaces that could make use of ACT common modules and started discussions with potential transition partners on transition paths to those applications. - Initiated discussions to specify the configuration of the independent government evaluation at the end of the program Phase I. - Conducted Preliminary Design Review (PDR) of ACT Common Module designs. ***FY 2015 Plans:*** - Continue development of application specific integrated circuits (ASIC) in 32 nanometer (nm) CMOS, 65 nm CMOS and Silicon Germanium (SiGe) technologies that enable both commonality across a wide range of platforms and elemental level digital beamforming, the combination of which results in lower cost and faster technology refresh of phased array antenna platforms. - Continue development and integration of common hardware components for a wide range of phased array antenna systems such as application specific integrated circuits, field programmable gate arrays, high data rate, low energy digital buses, high speed connectors, high isolation printed circuit boards, and waste heat removal technologies. - Finalize test plan for independent government common module testing.			

C. Accomplishments/Planned Programs ($ in Millions)	FY 2014	FY 2015	FY 2016
- Continue the development of EM interface elements capable of reconfiguring for various array use cases and operational specifications, and demonstrate tuning over an octave of bandwidth and over multiple polarization settings. - Continue to demonstrate reconfigurability of EM interface components for various array performance specifications, and demonstrate compatibility with common digital back-end. - Continue to identify government application spaces and transition paths for the ACT Common Module and reconfigurable antenna apertures. - Conduct Critical Design Review (CDR) of ACT Common Module design. ***FY 2016 Plans:*** - Demonstrate the functionality of the common module in a bench-top, laboratory environment. - Demonstrate Common Module hardware viability through government testing of delivered hardware components in a government furnished system platform. - Investigate the benefits of and develop plans and preliminary designs for upgrading the ACT Common Module in a state-of-the-art fabrication process. - Demonstrate an RF switch, tunable component, or other basic component that will be incorporated into the pixelated array face. - Define the characterization of a switch, tunable component, or other component that is the basis of the antenna system, and create a comprehensive list of projected personalities available from this design. - Continue to identify government application spaces and transition paths for the ACT Common Module and reconfigurable antenna apertures.			
Title: Vanishing Programmable Resources (VAPR) ***Description:*** The Vanishing Programmable Resources (VAPR) program will create microelectronic systems capable of physically disappearing (either in whole or in part) in a controlled, triggerable manner. The program will develop and establish an initial set of materials and components along with integration and manufacturing capabilities to undergird a fundamentally new class of electronics defined by their performance and transience. These transient electronics ideally should perform in a manner comparable to Commercial Off-The-Shelf (COTS) systems, but with limited device persistence that can be programmed, adjusted in real-time, triggered, and/or sensitive to the deployment environment. Applications include sensors for conventional indoor/outdoor environments (buildings, transportation, and materiel), environmental monitoring over large areas, and simplified diagnosis, treatment, and health monitoring in the field. VAPR will explore transience characteristics of electronic devices and materials as well as build out an initial capability to make transient electronics a deployable technology for the DoD and Nation. The technological capability developed through VAPR will be demonstrated through a final test vehicle of a transient beacon. The beacon will serve as an application vehicle showing the manufacturability of the research and process developed in the VAPR program being performed in PE 0601101E, Project TRS-01. The beacon is meant to be functional on its own, but also a leading indicator of the types of circuits possible under the VAPR program.	9.645	5.500	3.000

Exhibit R-2, RDT&E Budget Item Justification: PB 2016 Defense Advanced Research Projects Agency	**Date:** February 2015
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*

C. Accomplishments/Planned Programs ($ in Millions)	**FY 2014**	**FY 2015**	**FY 2016**
To manufacture transient systems at scale will require significant research and development into: higher levels of circuit integration and complexity to realize advanced circuit functionalities; integrated system designs to achieve required function (in modes that offer programmed or triggered transience); integration of novel materials into circuit fabrication processes; and development of new packaging strategies. The efficacy of the technological capability developed through VAPR will be demonstrated through a final test vehicle of a transient sensor system. The goal is to develop a suite of design principles, develop strategies and pathways, process flows, tools and basic components that are readily generalizable and can be leveraged towards the development of many other transient electronics devices. ***FY 2014 Accomplishments:*** - Began developing foundry fabrication of transient electronics with key functions (RF, memory, digital logic, power supply, etc.). - Began developing increased circuit integration and complexity to implement advanced functionalities. - Initiated transient sensors and power supply strategy development. - Began developing transient device fabrication approaches. - Initiated transience mode demonstration in test vehicles. ***FY 2015 Plans:*** - Achieve a transience time of less than or equal to 5 minutes for simple electronic devices. - Reduce the variability of transience time to less than or equal to 90 seconds for simple electronic devices. - Demonstrate capability to have reliable operation of simple transient electronic devices for greater than 24 hours after deployment, with subsequent controlled transience. ***FY 2016 Plans:*** - Complete integration of transient devices and materials to form fully functional microsystems. - Achieve a transience time of less than or equal to 30 seconds for transient sensors with RF link. - Improve the variability of transience time to less than or equal to 10 seconds. - Realize reliable operation of transient microsystems for greater than 100 hours after deployment, with subsequent controlled transience.			
Title: Direct SAMpling Digital ReceivER (DISARMER) ***Description:*** The goal of the Direct SAMpling Digital ReceivER (DISARMER) program is to produce a hybrid photonic-electronic analog-to-digital converter (ADC) capable of coherently sampling the entire X-band (8-12 GigaHertz (GHz)). Conventional electronic wideband receivers are limited in dynamic range by both the electronic mixer and the back-end digitizers. By employing an ultra-stable optical clock, the DISARMER program will allow for mixer-less digitization and thereby improve the dynamic range	2.000	2.000	1.000

Exhibit R-2, RDT&E Budget Item Justification: PB 2016 Defense Advanced Research Projects Agency	Date: February 2015
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*

C. Accomplishments/Planned Programs ($ in Millions)	FY 2014	FY 2015	FY 2016
100x over the state of the art. Such a wide bandwidth, high fidelity receiver will have applications in electronic warfare and signals intelligence systems while dramatically reducing the cost, size and weight of these systems. The DISARMER program will develop a low jitter mode-locked laser to be used as the sampling source. The program will also develop a novel photonic processor chip on a silicon platform capable of hybrid electronic-photonic track-and-hold functionality and coherent photo-detection. These silicon photonic integrated circuits will be integrated with complementary metal-oxide semiconductor (CMOS) driver circuits and packaged for integration in the full DISARMER system. This program has advanced technology development efforts funded in PE 0603739E, Project MT-15. ***FY 2014 Accomplishments:*** - Completed research culminating in the design of a photonic processor chip incorporating waveguides, optical phase shifter and balanced photo-detectors. - Demonstrated initial mode locked laser design operating at 8 GHz repetition rate with < 5 fs of integrated timing jitter. ***FY 2015 Plans:*** - Incorporate micro-ring resonator into mode-locked laser design to further reduce jitter. - Fabricate and test the building blocks of the photonic processor, including high-speed, high-power photodetectors and 90 degree phase shifters. - Package photonic processor chip and electronic integrated circuit chip to achieve low parasitic capacitance and inductance between the two chips. ***FY 2016 Plans:*** - Finalize fabrication and packaging of temperature stable laser module capable of 8 GHz repetition rate, 1 ps pulse width, and < 5 fs of integrated timing jitter.			
Title: Hyper-wideband Enabled RF Messaging (HERMES)* ***Description:*** *Formerly Gargoyle Modern weapons systems are dependent on radio frequency (RF) links for communications, command and control of unmanned vehicles, GPS signals and battle management. This dependence will only grow with the move to disaggregated systems in the battlefield. Spectral allocations for these critical RF links confine operations to narrow bands that can be disrupted with commercial hardware. To create assured RF links in the congested battlefield, HERMES will study the architectures and develop the technologies to enable links with 10 GHz of instantaneous bandwidth >40 dB of processing gain. This program will explore the limits of	-	2.000	3.000

Exhibit R-2, RDT&E Budget Item Justification: PB 2016 Defense Advanced Research Projects Agency	**Date:** February 2015
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*

C. Accomplishments/Planned Programs ($ in Millions)	**FY 2014**	**FY 2015**	**FY 2016**
processing gain and the potential for tunable filtering within the band to remove narrow-band jammers. HERMES addresses two technical areas covering electronic and hybrid electronic-photonic solutions. ***FY 2015 Plans:*** - Perform analysis and simulation of frequency-dependent channel propagation effects with associated mitigation methods; define the operational envelope and constraints for such a system to include representative electromagnetic background environments, friendly and enemy interferers and multiuser operational environments. - Define system architecture to include wireless RF transmitter and receiver architectures with specifications flowed down to the subsystem and component level. ***FY 2016 Plans:*** - Develop and test photonic-enabled wideband receivers for future scaling of link technologies with overall reduction of the system size, weight and power (SWaP). - Demonstrate a prototype broadband wireless communication link with 10 GHz of instantaneous bandwidth.			
Title: Fast and Big Mixed-Signal Designs (FAB) ***Description:*** Developing capabilities to intermix and tightly integrate silicon processes which are currently supported at different scaling nodes and by different vendors is critical to increasing the capabilities of high-performance military microelectronics. For example, silicon-germanium (SiGe) Bipolar Complementary Metal Oxide Semiconductor (BiCMOS) processes allow CMOS logic to be integrated with radio frequency (RF) heterojunction bipolar transistors (HBTs), which enables mixed-signal circuits having RF analog capabilities tightly coupled to digital processing. However, the SiGe process flow was developed to integrate to a single CMOS technology node and significant design and engineering effort is required to retarget the flow for a new node. Thus, BiCMOS processes tend to lag behind commercial CMOS by several generations. This program will investigate the potential for a truly process-agnostic integration technology that is inclusive of any current or future circuit fabrication technology such as GaAs, GaN and SiGe with a standardized interconnect topology. Such a technology platform will enable the design of individual circuit IP blocks, such as low-noise amplifiers and analog-to-digital converters, with a goal of re-use of the intellectual property (IP) across applications. Re-use will allow the DoD to amortize the upfront design cost of these blocks over several designs instead of leveling the burden on a single program. Furthermore, the IP can be designed in the fabrication process best suited for the performance goals and evolve more quickly than larger, more expensive single chip systems-on-a-chip. Through standardization of the interface, FAB will enable the DoD to leverage the advancements driven by the global semiconductor market rather than relying on a single on-shore foundry provider or on proprietary circuit designs owned by a handful of traditional prime performers.	-	4.000	10.800

Exhibit R-2, RDT&E Budget Item Justification: PB 2016 Defense Advanced Research Projects Agency	Date: February 2015
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*

C. Accomplishments/Planned Programs ($ in Millions)	FY 2014	FY 2015	FY 2016
In the Applied Research part of this program, focus will be placed on the rapid development and insertion of microsystems utilizing SiGe technology with 14nm Si CMOS. The development of a SiGe fabrication process integrated with 14 nanometer Silicon CMOS will be explored. This program has advanced technology development efforts funded in PE 0603739E, Project MT-15. ***FY 2015 Plans:*** - Determine the best choices for the RF and digital technologies and the best methods of co-integration (monolithic, through-silicon via (TSV)s, interposer, etc.) in order to achieve program objectives, along with identifying partner(s) for fabrication and/or integration. - Begin circuit design activities to determine performance benefits of new processes enabled by the program. - Study the best technology for various RF functional blocks for optimal use of mixed technologies. ***FY 2016 Plans:*** - Continue to investigate choices for the RF and digital technologies and the best methods of co-integration (monolithic, through-silicon via (TSV)s, interposer, etc.) in order to achieve program objectives, along with identifying partner(s) for fabrication and/or integration. - Continue circuit design activities to determine performance benefits of new processes enabled by the program. - Continue to study the best technology for various RF functional blocks for optimal use of mixed technologies.			
Title: Direct On-Chip Digital Optical Synthesis (DODOS) ***Description:*** The development of techniques for precise frequency control of RF and microwave radiation in the 1940's revolutionized modern warfare. Frequency control is the enabling technology for RADAR, satellite and terrestrial communications, and positioning and navigation technology, among many other core DoD capabilities. By comparison, frequency control at optical frequencies is relatively immature, comparable to the state-of-the-art of microwave control in the 1930's. The first practical demonstration of optical frequency synthesis, utilizing a self-referenced optical comb, was performed in 1999 and, since that time, the precision and accuracy of optical measurements has improved by four orders of magnitude, including the demonstration of atomic clocks utilizing optical-frequency atomic transitions that far outperform existing technology based on microwave transitions. To date, however, optical frequency control has been constrained to laboratory experiments due to the large size, relative fragility, and high cost of optical comb-based synthesizers. Recent developments in self-referenced optical frequency combs in microscale resonators enable the development of a fully-integrated chip-scale optical frequency synthesizer. Ubiquitous low-cost robust optical frequency synthesis is expected to create a similar disruptive capability in optical technology as microwave frequency synthesis did in the 1940's, enabling high-bandwidth coherent optical communications, coherent synthesized-aperture LiDAR, portable high-accuracy atomic clocks, high-resolution standoff gas/toxin detection, and intrusion detection, among other foreseen applications.	-	3.000	8.000

Exhibit R-2, RDT&E Budget Item Justification: PB 2016 Defense Advanced Research Projects Agency	Date: February 2015
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*

C. Accomplishments/Planned Programs ($ in Millions)	FY 2014	FY 2015	FY 2016
The Direct On-chip Digital Optical Synthesis (DODOS) program will integrate a diverse range of photonic and electronic components to create a microscale, high-accuracy optical frequency synthesizer, in a compact, robust package, suitable for deployment in a wide variety of mission-critical DoD applications. Significant challenges in the program include the integration of heterogeneous devices and materials that are incompatible with conventional high-volume manufacturing of integrated circuits, optimizing efficient on-chip pump lasers and high-bandwidth detectors, and developing high-precision microwave control electronics with low power consumption. Basic research for this program is funded within PE 0601101E, Project ES-01. ***FY 2015 Plans:*** - Initiate design of DODOS system architecture. - Prototype and test high-bandwidth optical comb sources. - Prototype and test widely-tunable output laser sources. ***FY 2016 Plans:*** - Develop DODOS system architectures and integration approaches. - Validate device-level performance requirements, such as the control-loop bandwidths and optical link budget, needed to reach the DODOS program metrics at the system level. - Prototype critical photonic components in processes consistent with subsequent co-integration.			
Title: High power Amplifier using Vacuum electronics for Overmatch Capability (HAVOC) ***Description:*** The effectiveness of combat operations across all domains increasingly depends on our ability to control, exploit, and deny our adversaries use of the electromagnetic (EM) spectrum. The future ability to control the spectrum and deliver non-kinetic effects requires the development of advanced electronic components. HAVOC seeks to strengthen and maintain our dominance of the EM spectrum and overmatch rapidly emerging threats by providing unprecedented electronic attack capabilities by developing a wideband and agile waveform high-power vacuum amplifier. The size, weight, and power (SWaP) will be consistent with reusable airborne and mobile platforms enabling an increased offset range and the ability to engage multiple targets at the speed of light with minimal collateral damage. Realization of high power vacuum-electronic amplifier technology will require significant advancements in high current-density, long-life cathodes, wide band interaction circuits, high-power drivers, low-loss RF windows, and advanced power supplies. Such an electronic component will also bring new capabilities to air, ground, and ship-based radar systems. ***FY 2016 Plans:*** - Initiate the design of a wide-bandwidth, high power microwave vacuum electronic amplifier and identify specific component performance parameters and engineering tradeoffs. - Design, fabricate, and test high current-density cathodes capable of producing beam current consistent with amplifier output power requirements.	-	-	12.000

Exhibit R-2, RDT&E Budget Item Justification: PB 2016 Defense Advanced Research Projects Agency	Date: February 2015
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*

C. Accomplishments/Planned Programs ($ in Millions)	FY 2014	FY 2015	FY 2016
- Design, fabricate, and test wide bandwidth interaction structures with high beam-wave interaction efficiency and high power handling capability. - Design, fabricate, and test wide bandwidth vacuum windows with high power handling capability. - Investigate new magnetic materials and magnet configurations that enable compact, integrated beam focusing and transport architectures.			
Title: Next Generation Atomic Clock (NGAC) ***Description:*** Atomic clock technology provides the high-performance backbone of timing and synchronization for DoD navigation, communications, Intelligence Surveillance and Reconnaissance (ISR), and Electronic Warfare (EW) systems. Prior DARPA investment in Chip-Scale Atomic Clock (CSAC) technology has led to recent demonstrations of enhanced DoD capabilities, enabled by the wide availability of atomic-quality timing in portable battery-powered applications. The Next-Generation Atomic Clock (NGAC) program will develop a next-generation chip-scale atomic clock, with 100X-1000X improvement in key performance parameters, by employing alternative approaches to atomic confinement and interrogation, with particular focus on developing the component technologies necessary to enable low-cost manufacturing and robust deployment in harsh DoD environments. NGAC will develop chip-scale atomic clocks achieving temperature coefficient of frequency of 10^-15/degrees Celsius and drift < 10^-12/month. This will enable precise timing on low cost, size, weight, and power (CSWaP) platforms with extended mission duration. In order to achieve these performance metrics, new enabling technology and interrogation techniques will be integrated into systems and proven to operate on a moving platform. Basic research for this program is funded within PE 0601101E, Project ES-01. ***FY 2016 Plans:*** - Demonstrate prototype clock operation utilizing low-CSWaP component technology. - Evaluate environmental sensitivity, particularly temperature and acceleration. - Identify technology gaps and complete a roadmap for NGAC development.	-	-	8.400
Title: Precise Robust Inertial Guidance for Munitions (PRIGM) ***Description:*** The Precise Robust Inertial Guidance for Munitions (PRIGM) program will develop low-Cost, Size, Weight, and Power (CSWaP) inertial sensor technology for GPS-free munitions guidance. PRIGM comprises two focus areas: 1) Development of a Navigation-Grade Inertial Measurement Unit (NGIMU) that transitions state-of-the-art MEMS to DoD platforms by 2020; and 2) Research and development of Advanced Inertial MEMS Sensors (AIMS) to achieve gun-hard, high-bandwidth, high dynamic range navigation requirements with the objective of complete autonomy in 2030. PRIGM will advance state-of-the-art MEMS gyros from TRL-3 devices to a TRL-6 transition platform (complete IMU) that enables Service Labs to perform TRL-7 field demonstrations. PRIGM will exploit recent advances in heterogeneous integration of photonics and CMOS and advanced	-	-	10.000

C. Accomplishments/Planned Programs ($ in Millions)	FY 2014	FY 2015	FY 2016
MEMS technology to realize novel inertial sensors for application in extreme dynamic environments and beyond navigation-grade performance. High-dynamics navigation applications, such as smart munitions, require low-CSWaP inertial sensors demonstrating high bandwidth, high precision, and high shock tolerance. Conventional MEMS inertial sensors rely on capacitive sensing to measure position, which suffers from large parasitics, temperature sensitivity, and gas damping from narrow gaps. While various methods have been used to overcome challenges with capacitive readout, optical sensing has demonstrated potential for high sensitivity, low noise, and robust inertial sensing. Recent advances in heterogeneous integration, on-chip optical waveguides, and quantum-assisted sensing and readout demonstrate potential for optically interrogated MEMS enabled gyros/accelerometers (OMEGA), interferometric and resonant photonic waveguide optical gyros (iWOG/rWOG), and whole angle gyros (WAG) that reach fundamental measurement limits. Fully integrated opto-MEMS inertial sensors may comprise stiffer mechanical structures that are thus capable of higher shock, vibration, and temperature tolerance along with improved navigation performance. Advanced research for the program is budgeted in PE 0603739E, Project MT-15. ***FY 2016 Plans:*** - Model and design architectures for chip-scale optical gyroscopes based on waveguide technologies - Design and fabricate heterogeneously-integrated, chip-scale waveguide optical gyroscopes - Demonstrate high-bandwidth (100,000 degrees/s) inertial sensors - Model and design optically interrogated MEMS inertial sensors - Develop co-fabrication processes to support MEMS optical interrogation - Demonstrate shock survivability of sensors and component technologies			
Title: Near Zero Energy RF and Sensor Operations (N-ZERO) ***Description:*** The DoD has an unfilled need for a persistent, event driven sensing capability, where physical, electromagnetic and other sensors can be pre-placed and remain dormant until awoken by an external trigger or stimulus. State-of-the-art (SOA) sensors use active electronics to monitor the environment for the external trigger. The power consumed by these electronic circuits limits the sensor lifetime to durations of weeks to months. The Near Zero Power RF and Sensor Operations (N-ZERO) program will extend the lifetime of remotely deployed sensors from months to years. N-ZERO will develop the underlying technologies and demonstrate the capability to continuously and passively monitor the environment and wake-up an electronic circuit upon detection of a specific signature or trigger. Thereafter, sensor lifetime will be limited only by processing and communications of confirmed events or ultimately by the battery self-discharge. The Near Zero Energy RF and Sensor Operations (N-ZERO) program will replace the power consuming electronic circuits used for processing and detection of information in current systems with passive or extremely low energy devices. The N-	-	-	4.500

Exhibit R-2, RDT&E Budget Item Justification: PB 2016 Defense Advanced Research Projects Agency	Date: February 2015
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*

C. Accomplishments/Planned Programs ($ in Millions)	FY 2014	FY 2015	FY 2016
ZERO program will develop RF communications and physical sensor systems that collect, process, and detect the presence of useful information, while rejecting spurious signals and noise, using only the energy in the collected information to perform these functions. This will eliminate or significantly reduce the standby power consumption from the battery. By doing so, the N-ZERO program will provide the warfighter with wireless communications and sensors systems with massively reduced size and drastically increased mission life. The basic research component of this program is budgeted under PE 0601101E, Project ES-01. ***FY 2016 Plans:*** - Initiate development of hardware components enabling passive or near zero energy collection, processing and detection of communications and sensor information. - Initiate development of RF and physical sensor microsystems that collect, processes and detect the presence of desired signals while consuming near zero power. - Identify government application spaces and transition paths that will make use of N-ZERO signal processing and detection.			
Title: Microwaves and Magnetics (M&M) ***Description:*** Passive magnetic components such as frequency selective limiters (FSL), isolators, circulators, phase shifters and filters are integral to numerous military electronic systems in applications including radar, imaging, communications, and electronic warfare. However, the rate of development and level of integration in microwave and mm-wave magnetic components have severely lagged the corresponding advancements and monolithic integration of semiconductor, microelectromechanical systems (MEMS), and optical active devices. In some cases the magnetic technologies have changed little in the past 20 to 30 years. The Microwaves and Magnetics program will leverage advanced magnetic components leading to disruptive improvements in system performance and novel functionality; and it will drive advances in materials science, materials processing, and in component design, modeling, integration, and fabrication leading to disruptive technologies that will ensure control of the electromagnetic (EM) spectrum. This targeted program in advanced and integrated RF/microwave magnetic components will enable the improvements needed for the next generation of DoD electronic systems. This program has advanced technology development efforts funded in PE 0603739E, Project MT-15. ***FY 2016 Plans:*** - Investigate recent advances in magnetic materials science to identify new processing, fabrication, and integration techniques that can enable microwave components with reduced loss, increased bandwidth, and enhanced tunability. - Leverage new microwave component design and modeling techniques to assess the performance of advanced magnetic materials in microwave circuits and applications. - Initiate the design and development of magnetic components using advanced magnetic materials with reduced loss, increased bandwidth, and enhanced tunability.	-	-	5.000
Title: MultiPLEX	-	-	8.000

Exhibit R-2, RDT&E Budget Item Justification: PB 2016 Defense Advanced Research Projects Agency	Date: February 2015
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*

C. Accomplishments/Planned Programs ($ in Millions)	FY 2014	FY 2015	FY 2016
Description: Dominance of the electromagnetic spectrum is a central pillar of modern warfare. As carrier frequencies of signals continue to increase, our traditional RF systems encounter difficulties with capturing and processing them. Capturing wide swaths of the spectrum simultaneously using traditional electronic technology is too large and too power hungry for virtually any DoD platform. Photonic technology has reached a maturity where it can offer a solution by providing low-loss, chip-scale components with the necessary linearity and noise figure that RF systems demand. MultiPLEX will deliver a chip-scale channelized receiver covering 20 - 50 GHz in 200 MHz-wide channels with 12 effective bits of resolution. The program will focus on the design and build of a hybrid electronic-photonic system that encompasses the entire receiver, from the low noise amplifier to the analog-to-digital converter. The program will develop high-Q optical filters and on-chip photonic mixing with high spur free dynamic range. The fully integrated channelized receiver will impact signals intelligence and electronic warfare systems and demonstrate the feasibility and utility of integrated photonics for RF applications. ***FY 2016 Plans:*** - Design and simulate the complete channelized receiver and generate flow down specifications to component technologies. - Demonstrate the high risk photonic components in a high yield, repeatable fabrication process compatible with silicon manufacturing.			
Title: Diamond Enhanced Devices (DiamEnD) ***Description:*** Diamond Enhanced Devices (DiamEnD) will further unlock the potential of Gallium Nitride (GaN) High-electron-mobility transistors (HEMTs) in defense electronics by removing the thermal limitation on performance through replacement of the original substrate with high conductivity (optical quality) diamond. Today, state-of-the-art (SoA) GaN HEMTs used in monolithic microwave integrated circuits (MMICs) reside on moderate thermal conductivity Silicon Carbide (SiC) substrates, which thermally limit the linear power density to between 5 W/mm and 7 W/mm, well below the ultimate limits achieved in pulsed power RF experiments. Through the incorporation of diamond as the substrate and subsequent increase in transistor drain voltage, this linear power density can be boosted to 15-25 W/mm in devices with existing SoA GaN epitaxy layer and as high as 40-60 W/mm with further epitaxial material and transistor development. These DiamEnD devices can then be used to substantially increase output power or reduce system Size, Weight, and Power (SWAP). This increased power density will be the heart of future long range RF engagements, either for smaller systems using the increased power density in a small aperture, or by larger systems which will be able to engage at even longer ranges or faster search speeds. ***FY 2016 Plans:*** - Demonstrate that GaN epitaxy can be harvested from the SOA GaN on SiC epitaxy developed in the Wide Band Gap Semiconductors (WBGS)-RF program and mated with diamond substrates. - Initiate effort to develop the diamond substrate materials and transistor technology to demonstrate GaN on Diamond devices with up to 25 W/mm.	-	-	6.000

C. Accomplishments/Planned Programs ($ in Millions)	FY 2014	FY 2015	FY 2016
- Initiate effort to modify GaN epitaxy and modify transistor structures to have GaN material that can be used to make devices that can reach 40-60 W/mm.			
Title: Micro-Technology for Positioning, Navigation, and Timing (Micro PN&T)	19.736	13.500	-
Description: The Micro-Technology for Positioning, Navigation, and Timing (Micro-PNT) program is developing low-Cost, Size, Weight, and Power (CSWaP) inertial sensors and timing sources for navigation in GPS degraded environments, primarily focusing on the development of miniature solid state and atomic gyroscopes and clocks. Both classes of sensors are currently unsuitable for small platform or dismount soldier applications. Micro Electro-Mechanical Systems (MEMS) sensors have limited performance but excellent CSWaP, while atomic sensors are capable of excellent performance but are limited to laboratory experiments due to complexity and high CSWaP. Micro-PNT is advancing both technology approaches by improving the performance of MEMS inertial sensors and by miniaturizing atomic devices. Ultimately, low-CSWaP inertial sensors and clocks will enable ubiquitous guidance and navigation on all platforms, including guided munitions, unmanned aerial vehicles (micro-UAVs), and mounted and dismounted soldiers. The successful realization of Micro-PNT depends on the development of new microfabrication processes and novel material systems for fundamentally different sensing modalities, as well as understanding the error sources at the microscale and the scaling relationships for size reduction of sensors based on atomic physics techniques. The Micro-PNT program includes research into novel techniques for fabrication and integration of three-dimensional MEMS devices as well as theoretical and experimental studies of new architectures and geometries for MEMS inertial sensing. Atomic physics research includes the development of new architectures for atomic inertial sensing and investigation of miniature enabling technologies, whose conventional counterparts are currently large, power hungry, and temperature sensitive, limiting high performance sensors to laboratory demonstrations. Advanced research for the program is budgeted in PE 0603739E, Project MT-12. ***FY 2014 Accomplishments:*** - Demonstrated rotational sensitivity of prototype miniature inertial sensors based on modern atomic physics techniques. - Demonstrated pulsed nuclear magnetic resonance gyroscopes. - Demonstrated electronic and algorithmic self-calibration of MEMS gyroscopes to achieve better than 100 ppm long-term stability of scale factor and bias. - Demonstrated a three-axis MEMS inertial sensor with total device volume < 10 mm^3. - Explored novel, enabling technologies for atom physics based devices (ex: magnet-free ion pump, shutter technology, alkali vapor pressure control). ***FY 2015 Plans:*** - Demonstrate on-chip MEMS calibration stages to track bias and scale factor stability repeatable to <100 ppm. - Demonstrate a miniaturized, low-drift Nuclear Magnetic Resonance (NMR) gyroscope.			

C. Accomplishments/Planned Programs ($ in Millions)	FY 2014	FY 2015	FY 2016
- Fabricate low loss shell resonators for gyroscope applications with ringdown time > 100 seconds. - Demonstrate novel, enabling technologies for atom physics based devices (ex: magnet-free ion pump, shutter technology, alkali vapor pressure control)			
Title: Terahertz Electronics ***Description:*** The Terahertz Electronics program is developing the critical semiconductor device and integration technologies necessary to realize compact, high-performance microelectronic devices and circuits that operate at center frequencies exceeding 1 Terahertz (THz). There are numerous benefits for electronics operating in the THz regime and new applications in imaging, radar, communications, and spectroscopy. The Terahertz Electronics program is divided into two major technical activities: Terahertz Transistor Electronics that includes the development and demonstration of materials and processing technologies for transistors and integrated circuits for receivers and exciters that operate at THz frequencies; and Terahertz High Power Amplifier Modules that includes the development and demonstration of device and processing technologies for high power amplification of THz signals in compact modules. ***FY 2014 Accomplishments:*** - Completed circuit demonstrations between 0.67 THz and 0.85 THz, including high power amplifiers and integrated circuits. - Improved process yield of 0.67 THz transistors and demonstrated key building blocks for 0.67 THz heterodyne detectors and sensors. - Completed design and initiated fabrication of a 1.03 THz vacuum amplifier. - Demonstrated world's first THz Monolithic Microwave Integrated Circuit (MMIC) amplifier, which produced 10dB of gain at 1.0 THz. ***FY 2015 Plans:*** - Complete measurements of receiver/exciter technologies at and above 0.67 THz. - Demonstrate oscillator circuits at 1.03 THz. - Demonstrate prototype THz transceiver link using THz Indium Phosphide (InP) technology. - Demonstrate a 1.03 THz vacuum amplifier. - Demonstrate improved thermal performance of vacuum amplifier for high duty cycle operation at THz frequencies.	14.250	8.020	-
Title: Nitride Electronic NeXt-Generation Technology (NEXT) ***Description:*** To realize high performance analog, Radio Frequency (RF) and mixed-signal electronics, a next-generation transistor technology with high cutoff frequency and high breakdown voltage is under development. This technology will enable large voltage swing circuits for military applications that the current state-of-the-art silicon transistor technology cannot support. The objective of the NEXT program is to develop a revolutionary, wide band gap, nitride transistor technology that simultaneously provides extremely high-speed and high-voltage swing [Johnson Figure of Merit (JFoM) larger than 5 Terahertz (THz)-V] in a	7.480	4.280	-

Exhibit R-2, RDT&E Budget Item Justification: PB 2016 Defense Advanced Research Projects Agency	Date: February 2015
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*

C. Accomplishments/Planned Programs ($ in Millions)	FY 2014	FY 2015	FY 2016
process consistent with large scale integration of enhancement/depletion (E/D) mode logic circuits of 1,000 or more transistors. In addition, this fabrication process will be reproducible, high-yield, high-uniformity, and highly reliable. The accomplishment of this goal will be validated through the demonstration of specific program Process Control Monitor (PCM) Test Circuits such as 5, 51 and 501-stage ring oscillators in each program phase. The impact of this next-generation nitride electronic technology will be the speed, linearity, and power efficiency improvement of RF and mixed-signal electronic circuits used in military communications, electronic warfare and sensing. ***FY 2014 Accomplishments:*** - Completed enhancement / depletion mode transistor scaling development for fully self-aligned nitride transistors with full process compatibility. - Initiated development of NEXT process design kit for circuit designers. - Designed and fabricated RF signal demonstration circuits based on latest NEXT transistors and integration processes. ***FY 2015 Plans:*** - Establish the baseline of the high-speed / high breakdown voltage NEXT fabrication technology with high reproducibility and yield. - Design, fabricate, and test military-relevant circuits, such as RF power amplifiers, using the developed NEXT transistor technology. - Update NEXT process design kit to allow external circuit designers to utilize NEXT technology in other advanced circuit designs.			
Title: Microscale Plasma Devices (MPD) ***Description:*** The goal of the Microscale Plasma Devices (MPD) program is to design, develop, and characterize MPD technologies, circuits, and substrates. The MPD program will focus on development of fast, small, reliable, high-carrier-density, micro-plasma switches capable of operating in extreme conditions, such as high-radiation and high-temperature environments. Specific focus will be given to methods that provide efficient generation of ions that can perform robust signal processing of radio frequency (RF) through light electromagnetic energy over a range of gas pressures. Applications for such devices are far reaching, including the construction of complete high-frequency plasma-based circuits, and microsystems with superior resistance to radiation and extreme temperature environments. It is envisaged that both two and multi-terminal devices consisting of various architectures will be developed and optimized under the scope of this program. MPDs will be developed in various circuits and substrates to demonstrate the efficacy of different approaches. MPD-based microsystems are demonstrated in DoD applications where electronic systems must survive in extreme environments. The MPD applied research program is focused on transferring the fundamental scientific advances funded by PE 0601101E, Project ES-01 to produce complex circuit designs that may be integrated with commercial electronic devices. It is expected that	5.310	2.000	-

Exhibit R-2, RDT&E Budget Item Justification: PB 2016 Defense Advanced Research Projects Agency	Date: February 2015
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*

C. Accomplishments/Planned Programs ($ in Millions)	FY 2014	FY 2015	FY 2016
the MPD program will result in the design and modeling tools, as well as the fabrication capabilities necessary to commercially manufacture high-performance microscale-plasma-device-based electronic systems for advanced DoD applications. ***FY 2014 Accomplishments:*** - Continued integration of multiple simulation efforts into the modeling-and-simulation design tool (MSDT) for commercial development of microplasma based electronics and DoD systems. - Optimized plasma microcavity materials for DoD systems of interest, demonstrating robust electronic protection in high power electromagnetic environments. - Demonstrated and tested nonlinear signal processing circuit devices and architectures based on MPD technologies. ***FY 2015 Plans:*** - Complete integration of the simulation efforts into the MSDT for commercial development of microplasma based electronics. - Complete final testing of microcavity materials for robustness in a high power electromagnetic application in order to demonstrate a Technology Readiness Level (TRL) as needed for technology transition. - Complete demonstration of plasma-based materials and devices in representative system applications for transition to multiple DoD customers.			
Title: Micro-coolers for Focal Plane Arrays (MC-FPA) ***Description:*** The Micro-coolers for Focal Plane Arrays (MC-FPA) program will develop low Size, Weight, Power, and Cost (SWaP-C) cryogenic coolers for application in high performance IR cameras. The sensitivity of an IR focal-plane array (FPA) is improved by cooling its detectors to cryogenic temperatures. The disadvantages of state-of-the-art Stirling cryo-coolers used for high performance IR FPAs are large size, high power and high cost. On the other hand, thermoelectric (TE) coolers used in low performance IR cameras are relatively small, but are inefficient, and it is difficult to achieve temperatures below 200 Kelvin (K). To reduce IR camera SWaP-C, innovations in cooler technology are needed. This program will exploit the Joule-Thomson (J-T) cooling principle, in a silicon-based MEMS technology, for making IR FPA coolers with very low SWaP-C. MEMS microfluidics, piezoelectric MEMS, and complementary metal-oxide semiconductor (CMOS) electronics will be used to demonstrate an integrated cold head and compressor, all in a semiconductor chip. Since a J-T cooler works by cooling from gas expansion, the coefficient of performance is expected to be much higher than state-of-the-art TE coolers, while being significantly smaller than Stirling coolers. The chip-scale J-T cooler will be designed for pressure ratios of four or five to one with high compressor frequency in a small volume. The goal of the MC-FPA program will be to demonstrate cooling down to 150 K. The chip-scale micro-coolers will cost less and will be significantly smaller than current Stirling coolers. Once the proof-of-principle is demonstrated, the subsequent program effort will focus on transitioning to chip-scale manufacture on eight to twelve inch wafers, resulting in cooler costs decreasing to as low as $50. An extended wavelength-range short-wave IR detector will	2.450	1.000	-

C. Accomplishments/Planned Programs ($ in Millions)	FY 2014	FY 2015	FY 2016
be integrated with a micro-cooler for demonstration of the MC-FPA. The basic research component of this program is budgeted under PE 0601101E, Project ES-01. ***FY 2014 Accomplishments:*** - Developed detector design for response in 1-2.4 micrometers. - Performed materials growth and characterization for detector fabrication. - Processed Cadmium Zinc Telluride (CdZnTe) substrates for epitaxy. - Completed initial analysis to determine input cell design for readout integrated circuit (ROIC). - Developed 640X480 extended shortwave infrared (1-2.4 micrometer cutoff) FPA. - Designed a readout integrated circuit (ROIC) for the IR FPA chip. - Demonstrated camera electronics for the FPA with provision for chip-scale micro-cooler. ***FY 2015 Plans:*** - Evaluate 3-stage J-T micro-cooler. - Hybridize FPA to ROIC, integrate 3-stage J-T micro-cooler, and test. - Evaluate 5-stage J-T micro-cooler. - Hybridize FPA to ROIC and integrate 5-stage J-T micro-cooler with complete backend packaging. - Complete camera integration and housing. - Complete camera tests and demo. - Final camera delivery and program close out.			
Title: Microscale Power Conversion (MPC) ***Description:*** Today's power amplifiers utilize large, bulky, independently designed fixed voltage power supplies that fundamentally limit RF system output power, power efficiency and potential for integration. The Microscale Power Conversion (MPC) program developed X-band RF transmitters as system-in-package modules, in which integrated circuit power amplifiers were integrated with dynamic, variable voltage power supplies using high-speed power switches. Such an integrated microsystem supports military applications requiring several hundred Megahertz (MHz) of RF envelope bandwidth at large peak-to-average power ratios. This integration approach realized RF systems with significantly higher overall power efficiency and waveform diversity by changing from fixed power supply architecture to dynamic power supply architecture. The program was structured in two technical tracks. The first track developed high-speed power switch technology to be used in the design of dynamic power supply and modulator circuits. The second track developed the simultaneous co-design and integration of the RF power amplifier and dynamic power supply circuits to achieve maximum overall power efficiency for the desired waveforms of interest. The program enabled increased deployment of MPC RF transmitter systems on DoD platforms due to their more compact size, high efficiency, lower lifecycle cost and enhanced RF performance enabling, for example, significantly communications rates.	8.800	-	-

Exhibit R-2, RDT&E Budget Item Justification: PB 2016 Defense Advanced Research Projects Agency	**Date:** February 2015
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*

C. Accomplishments/Planned Programs ($ in Millions)	**FY 2014**	**FY 2015**	**FY 2016**
FY 2014 Accomplishments: - Completed very high frequency, low-loss power switch technology for implementing large envelope-bandwidth modulators for RF power amplifiers. - Demonstrated final co-designs of advanced X-band transmitter including drain and gate bias modulation, dynamic output impedance matching, and closed-loop control with fast-switching power modulation. - Furnished power switch process design kits to DoD contractors for use in future power supply modulator or power amplifier designs.			
Title: Photonically Optimized Embedded Microprocessor (POEM) ***Description:*** Based upon current scaling trends, microprocessor performance is projected to fall far short of future military needs. Microprocessor performance is saturating and leading to reduced computational efficiency because of the limitations of electrical communications. The POEM program demonstrated chip-scale, silicon-photonic technologies that can be integrated within embedded microprocessors for seamless, energy-efficient, high-capacity communications within and between the processor chip and dynamic random access memory (DRAM) chip. This technology propelled microprocessors onto a higher performance trajectory by overcoming this "memory wall". ***FY 2014 Accomplishments:*** - Demonstrated a photonic link between two Silicon-on-Insulator-Complementary-metal-oxide-semiconductor (SOI-CMOS) DRAM chips consuming 1.3 (2.8) pJ/bit employing foundry-compatible photonic devices and respective control and driver circuits. - Fabricated and tested optical receiver circuits with 31 nanoseconds (ns) locking time and consuming 5.4 pJ/bit operating at 25 Gb/s. - Designed new algorithms that effectively parallelize graph analytic problems (e.g. community analysis and shortest path), taking advantage of the high bandwidth photonic interconnects. - Designed and optimized material stack for fabricating an on-chip, uncooled laser operating at 1550 nm with >7% wall plug efficiency at 80C.	1.500	-	-
Accomplishments/Planned Programs Subtotals	222.287	169.203	174.798

D. Other Program Funding Summary ($ in Millions)

N/A

Remarks

E. Acquisition Strategy

N/A

Exhibit R-2, **RDT&E Budget Item Justification:** PB 2016 Defense Advanced Research Projects Agency		**Date:** February 2015
Appropriation/Budget Activity 0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research*	**R-1 Program Element (Number/Name)** PE 0602716E / *ELECTRONICS TECHNOLOGY*	

F. Performance Metrics

Specific programmatic performance metrics are listed above in the program accomplishments and plans section.