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| **Appropriation/Budget Activity**<br>0400: *Research, Development, Test & Evaluation, Defense-Wide* / BA 2: *Applied Research* | **R-1 Program Element (Number/Name)**<br>PE 0602716E / *ELECTRONICS TECHNOLOGY* |

| COST ($ in Millions) | Prior Years | FY 2013 | FY 2014 | FY 2015 Base | FY 2015 OCO # | FY 2015 Total | FY 2016 | FY 2017 | FY 2018 | FY 2019 | Cost To Complete | Total Cost |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Total Program Element | - | 192.349 | 233.469 | 179.203 | - | 179.203 | 183.439 | 184.458 | 187.536 | 192.637 | - | - |
| ELT-01: *ELECTRONICS TECHNOLOGY* | - | 192.349 | 233.469 | 179.203 | - | 179.203 | 183.439 | 184.458 | 187.536 | 192.637 | - | - |

# The FY 2015 OCO Request will be submitted at a later date.

**A. Mission Description and Budget Item Justification**

This program element is budgeted in the Applied Research budget activity because its objective is to develop electronics that make a wide range of military applications possible.

Advances in microelectronic device technologies, including digital, analog, photonic and MicroElectroMechanical Systems (MEMS) devices, continue to have significant impact in support of defense technologies for improved weapons effectiveness, improved intelligence capabilities and enhanced information superiority. The Electronics Technology program element supports the continued advancement of these technologies through the development of performance driven advanced capabilities, exceeding that available through commercial sources, in electronic, optoelectronic and MEMS devices, semiconductor device design and fabrication techniques, and new materials and material structures for device applications. A particular focus for this work is the exploitation of chip-scale heterogeneous integration technologies that permit the optimization of device and integrated module performance.

The phenomenal progress in current electronics and computer chips will face the fundamental limits of silicon technology in the early 21st century, a barrier that must be overcome in order for progress to continue. Another thrust of the program element will explore alternatives to silicon-based electronics in the areas of new electronic devices, new architectures to use them, new software to program the systems, and new methods to fabricate the chips. Approaches include nanotechnology, nanoelectronics, molecular electronics, spin-based electronics, quantum-computing, new circuit architectures optimizing these new devices, and new computer and electronic systems architectures. Projects will investigate the feasibility, design, and development of powerful information technology devices and systems using approaches for electronic device designs that extend beyond traditional Complementary Metal Oxide Semiconductor (CMOS) scaling, including non silicon-based materials technologies to achieve low cost, reliable, fast and secure computing, communication, and storage systems. This investigation is aimed at developing new capabilities from promising directions in the design of information processing components using both inorganic and organic substrates, designs of components and systems leveraging quantum effects and chaos, and innovative approaches to computing designs incorporating these components for such applications as low cost seamless pervasive computing, ultra-fast computing, and sensing and actuation devices.

This project has five major thrusts: Electronics, Photonics, MicroElectroMechanical Systems, Architectures, Algorithms, and other Electronic Technology research.

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| B. Program Change Summary ($ in Millions) | FY 2013 | FY 2014 | FY 2015 Base | FY 2015 OCO | FY 2015 Total |
|---|---|---|---|---|---|
| Previous President's Budget | 222.416 | 243.469 | 254.104 | - | 254.104 |
| Current President's Budget | 192.349 | 233.469 | 179.203 | - | 179.203 |
| Total Adjustments | -30.067 | -10.000 | -74.901 | - | -74.901 |
| • Congressional General Reductions | -0.283 | - | | | |
| • Congressional Directed Reductions | -26.166 | -10.000 | | | |
| • Congressional Rescissions | - | - | | | |
| • Congressional Adds | - | - | | | |
| • Congressional Directed Transfers | - | - | | | |
| • Reprogrammings | 1.903 | - | | | |
| • SBIR/STTR Transfer | -5.521 | - | | | |
| • TotalOtherAdjustments | - | - | -74.901 | - | -74.901 |

**Change Summary Explanation**

FY 2013: Decrease reflects Congressional reductions for Sections 3001 & 3004 and directed reductions, sequestration adjustments, and the SBIR/STTR transfer offset by reprogrammings.

FY 2014: Decrease reflects a reduction for program growth.

FY 2015: Decrease reflects drawdown of several efforts prior to transition: Adaptive RF Technology, NEXT, Micro PNT, Microscale Power Conversion and POEM.

| C. Accomplishments/Planned Programs ($ in Millions) | FY 2013 | FY 2014 | FY 2015 |
|---|---|---|---|
| ***Title:*** Terahertz Electronics | 15.600 | 15.020 | 6.100 |

***Description:*** The Terahertz Electronics program is developing the critical semiconductor device and integration technologies necessary to realize compact, high-performance microelectronic devices and circuits that operate at center frequencies exceeding 1 Terahertz (THz). There are numerous benefits for electronics operating in the THz regime and new applications in imaging, radar, communications, and spectroscopy. The Terahertz Electronics program is divided into two major technical activities: Terahertz Transistor Electronics that includes the development and demonstration of materials and processing technologies for transistors and integrated circuits for receivers and exciters that operate at THz frequencies; and Terahertz High Power Amplifier Modules that includes the development and demonstration of device and processing technologies for high power amplification of THz signals in compact modules.

***FY 2013 Accomplishments:***

- Achieved key device and integration technologies to realize compact, high performance electronic circuits operating beyond 0.85 THz.

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| C. Accomplishments/Planned Programs ($ in Millions) | FY 2013 | FY 2014 | FY 2015 |
|---|---|---|---|
| - Developed key device and integration technologies to realize compact, high performance electronic circuits operating beyond 0.85 THz.<br>- Completed device, integration, and metrology technologies to enable the manufacture of microsystems, such as heterodyne detectors, between 0.67 and 0.85 THz for advanced communications and radar applications at sub-millimeter wave frequencies.<br>- Initiated multiple circuit implementations for applications between 0.67 THz and 0.85 THz, including passive structures required for signal handling at sub-mm-wave frequencies.<br>- Developed measurement techniques for verifying circuit capability above 0.85 THz and calibrated these methods in a laboratory environment.<br>***FY 2014 Plans:***<br>- Complete circuit demonstrations between 0.67 THz and 0.85 THz, including high power amplifiers and integrated circuits.<br>- Improve process yield of 0.67 THz transistors and demonstrate key building blocks for 0.67 THz heterodyne detectors and sensors.<br>- Complete design and initiate fabrication of a 1.03 THz vacuum amplifier.<br>***FY 2015 Plans:***<br>- Complete measurements of receiver/exciter technologies at and above 0.67 THz.<br>- Demonstrate oscillator circuits at 1.03 THz.<br>- Demonstrate prototype THz transceiver link using THz Indium Phosphide (InP) technology.<br>- Demonstrate improved thermal performance of vacuum amplifier for high duty cycle operation at THz frequencies. | | | |
| ***Title:*** Adaptive Radio Frequency Technology (ART)<br>***Description:*** There is a critical ongoing military need for flexible, affordable, and small size, weight and power (SWaP) real-time-adaptable military electromagnetic interfaces. The Adaptive Radio Frequency Technology (ART) program will provide the warfighter with a new, fully adaptive radio platform capable of sensing the electromagnetic and waveform environment in which it operates, making decisions on how to best communicate in that environment, and rapidly adapting its hardware to meet ever-changing requirements, while simultaneously significantly reducing the SWaP of such radio nodes. ART technology will also provide each warfighter, as well as small-scale unmanned platforms, with compact and efficient signal identification capabilities for next-generation cognitive communications, and sensing and electronic warfare applications. ART technology will also enable rapid radio platform deployment for new waveforms and changing operational requirements. The project will remove the separate design tasks needed for each unique Radio Frequency (RF) system, which will dramatically reduce the procurement and sustainment cost of military systems. ART aggregates the Feedback Linearized Microwave Amplifiers program, the Analog Spectral Processing program, and Chip Scale Spectrum Analyzers (CSSA) program, and initiates new thrusts in Cognitive Low-energy Signal Analysis and Sensing Integrated Circuits (CLASIC), and Radio-Frequency Field-Programmable Gate Arrays (RF-FPGA). | 25.494 | 26.949 | 20.423 |

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| C. Accomplishments/Planned Programs ($ in Millions) | FY 2013 | FY 2014 | FY 2015 |
|---|---|---|---|

***FY 2013 Accomplishments:***

- Demonstrated highly linear time delay unit monolithic microwave integrated circuit for beam-steering applications in wideband phased arrays.
- Demonstrated micro electro-mechanical systems (MEMS)-based channelized RF receiver topology for use in high-speed spectrum sensing applications from 0.02 - 6 gigahertz (GHz) with a scan rate > 5 terahertz per second.
- Demonstrated world's first signal classification application-specific integrated circuit for the purpose of signal classification. Power consumption is sufficiently low to allow 170 hours of continuous classification on a single charge of a typical smartphone battery.
- Demonstrated initial hardware implementations of developed signal recognition concepts/techniques.
- Demonstrated simulations of direction-of-arrival hardware with 1.7 picoJoule/operation, which is 2 orders of magnitude lower than conventional processors.
- Developed efficient and robust computer-aided design optimization algorithms for RF-FPGA programming including development of an emulation board for demonstrating these concepts.
- Demonstrated usage of MEMS switches for reconfiguration of piezoelectric resonators/filters.
- Demonstrated multi-channel filter manifold design showing the capability for switching resonators in and out of a filter for near-arbitrary transfer function control.
- Developed flexible and programmable hybrid phase-locked loop with frequency tuning range up to 19 GHz.
- Completed DC-to-20 GHz circuit for military applications, with both coarse- and fine-grained on-the-fly reconfigurability, all on a single monolithic integrated circuit fabricated in a commercial foundry process.
- Demonstrated novel phase change material switches for use in RF-FPGAs with insertion loss <0.15 dB out to 50 GHz and < 0.5 dB out to 100 GHz with isolation > -10 dB over the full 100 GHz.

***FY 2014 Plans:***

- Demonstrate reconfigurable RF circuit (RF-FPGA) technologies at the component and system levels along with the necessary computer-aided design approaches.
- Demonstrate the applicability of one RF hardware design for 5 different application spaces, as a prototype for how ART technology can lead the way to life-cycle cost reduction.
- Demonstrate advanced concepts for signal recognition at the hardware level and initiate plans for transitioning these approaches to relevant DoD systems.
- Demonstrate applicability of tunable filters for dynamic frequency allocation in a fielded radio system.

***FY 2015 Plans:***

- Demonstrate final circuit design technologies including microwave switches, frequency synthesis and RF functionality.

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| C. Accomplishments/Planned Programs ($ in Millions) | FY 2013 | FY 2014 | FY 2015 |
|---|---|---|---|
| - Demonstrate a fully reconfigurable RF filter element with serial addressing of the components in an appropriate package form factor.<br>- Optimize the RF phase-change switch technology and perform a final RF-FPGA demonstration.<br>- Implement transition plans for a fully reconfigurable RF circuit technology at the component and system levels. | | | |
| ***Title:*** Nitride Electronic NeXt-Generation Technology (NEXT)<br><br>***Description:*** To realize high performance analog, Radio Frequency (RF) and mixed-signal electronics, a next-generation transistor technology with high cutoff frequency and high breakdown voltage is under development. This technology will enable large voltage swing circuits for military applications that the current state-of-the-art silicon transistor technology cannot support. The objective of the Nitride Electronic neXt-generation Technology (NEXT) program is to develop a revolutionary, wide band gap, nitride transistor technology that simultaneously provides extremely high-speed and high-voltage swing [Johnson Figure of Merit (JFoM) larger than 5 Terahertz (THz)-V] in a process consistent with large scale integration of enhancement/depletion (E/D) mode logic circuits of 1000 or more transistors. In addition, this fabrication process will be reproducible, high-yield, high-uniformity, and highly reliable. The accomplishment of this goal will be validated through the demonstration of specific program Process Control Monitor (PCM) Test Circuits such as 5, 51 and 501-stage ring oscillators in each program phase. The impact of this next-generation nitride electronic technology will be the speed, linearity, and power efficiency improvement of RF and mixed-signal electronic circuits used in military communications, electronic warfare and sensing.<br><br>***FY 2013 Accomplishments:***<br>- Demonstrated world record, wide-bandgap nitride transistor technology with operation up to 450 GigaHertz (GHz) through scaling efforts for self-aligned structures with short gate length, novel barrier layers, and reduced parasitic elements.<br>- Increased the Technology Readiness Level (TRL) of the transistor fabrication process for future power switching and Monolithic Microwave Integrated Circuit (MMIC) capability using advanced wide band gap devices.<br>- Continued to improve the versatility and circuit design potential of the NEXT MMIC process by successfully integrating Schottky diodes.<br><br>***FY 2014 Plans:***<br>- Complete enhancement / depletion mode transistor scaling development for fully self-aligned nitride transistors with full process compatibility.<br>- Develop NEXT process development kit for circuit designers.<br>- Design and fabricate RF or mixed signal demonstration circuits based on latest NEXT transistors and integration processes.<br><br>***FY 2015 Plans:***<br>- Establish the baseline of the high-speed / high breakdown voltage NEXT fabrication technology with high reproducibility and yield. | 8.360 | 8.080 | 4.280 |

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| C. Accomplishments/Planned Programs ($ in Millions) | FY 2013 | FY 2014 | FY 2015 |
|---|---|---|---|
| - Design, fabricate, and test military-relevant circuits, such as RF power amplifiers, using the developed NEXT transistor technology.<br>- Complete NEXT process design kit to allow external circuit designers to utilize NEXT technology in other advanced circuit designs. | | | |
| ***Title:*** Diverse & Accessible Heterogeneous Integration (DAHI) | 27.153 | 34.385 | 33.400 |
| ***Description:*** Prior DARPA efforts have demonstrated the ability to monolithically integrate different semiconductor types to achieve near-ideal "mix-and-match" capability for DoD circuit designers. Specifically, the Compound Semiconductor Materials On Silicon (COSMOS) program enabled transistors of Indium Phosphide (InP) to be freely mixed with silicon complementary metal-oxide semiconductor (CMOS) circuits to obtain the benefits of both technologies (very high speed and very high circuit complexity/ density, respectively). The Diverse & Accessible Heterogeneous Integration (DAHI) effort will take this capability to the next level, ultimately offering the seamless co-integration of a variety of semiconductor devices (for example, Gallium Nitride, Indium Phosphide, Gallium Arsenide, Antimonide Based Compound Semiconductors), microelectromechanical (MEMS) sensors and actuators, photonic devices (e.g., lasers, photo-detectors) and thermal management structures. This capability will revolutionize our ability to build true "systems on a chip" (SoCs) and allow dramatic size, weight and volume reductions for a wide array of system applications.<br><br>In the Applied Research part of this program, high performance RF/optoelectronic/mixed-signal systems-on-a-chip (SoC) for specific DoD transition applications will be developed as a demonstration of the DAHI technology. To provide maximum benefit to the DoD, these processes will be transferred to a manufacturing flow and made available (with appropriate computer aided design support) to a wide variety of DoD laboratory, Federally Funded Research and Development Center (FFRDC), academic and industrial designers. Manufacturing yield and reliability of the DAHI technologies will be characterized and enhanced. This program has basic research efforts funded in PE 0601101E, Project ES-01, and advanced technology development efforts funded in PE 0603739E, Project MT-15.<br><br>***FY 2013 Accomplishments:***<br>- Continued fabrication and testing of higher complexity new generation of heterogeneously-integrated wideband, ultra-high-linearity analog-to-digital converters with in situ silicon-enabled calibration and linearization.<br>- Demonstrated ultra-wideband Analog-to-Digital Converter (ADC) with signal-to-noise-and-distortion ratio (SINAD) of over 30 Decibels (dB) at input frequencies of up to 20GHz with instantaneous bandwidth of 6GHz.<br>- Completed final multi-project wafer run of multi-user two-technology compound-semiconductor-on-silicon foundry process.<br>- Demonstrated a wide array of RF/mixed-signal components utilizing heterogeneous integration, including low-noise amplifiers, high-speed track-and-hold circuits, RF digital-to-analog converters, and tunable bandpass filters, which demonstrate the advantages of heterogeneous integration over single-technology integrated circuits. | | | |

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| C. Accomplishments/Planned Programs ($ in Millions) | FY 2013 | FY 2014 | FY 2015 |
|---|---|---|---|
| - Initiated new CMOS-compatible processes to achieve heterogeneous integration with multiple diverse types of compound semiconductor transistors, MEMS, and non-silicon photonic devices, including interconnect and thermal management approaches.<br>- Initiated manufacturing, yield and reliability enhancement for multi-user foundry capability based on developed diverse heterogeneous integration processes.<br>- Continued design and fabrication of high-complexity heterogeneously integrated RF/optoelectronic/mixed signal and circuits, such as wide band RF transmitters, advanced mixed-signal integrated systems, optoelectronic RF signal sources, and laser-radar chips.<br>***FY 2014 Plans:***<br>- Continue to develop new CMOS-compatible processes to achieve heterogeneous integration with diverse types of compound semiconductor transistors, MEMS, and non-silicon photonic devices, including interconnect and thermal management approaches.<br>- Continue manufacturing, yield and reliability enhancement for multi-user foundry capability based on developed diverse heterogeneous integration processes.<br>- Continue design and fabrication of high complexity heterogeneously integrated RF/optoelectronic/mixed signal and circuits, such as wide band RF transmitters, advanced mixed signal integrated systems, optoelectronic RF signal sources, and laser-radar systems.<br>***FY 2015 Plans:***<br>- Complete development of new CMOS-compatible processes to achieve heterogeneous integration with diverse types of compound semiconductor transistors, MEMS, and non-silicon photonic devices, including interconnect and thermal management approaches.<br>- Complete manufacturing, yield and reliability enhancement for multi-user foundry capability based on developed diverse heterogeneous integration processes.<br>- Complete design and fabrication of high complexity heterogeneously integrated RF/optoelectronic/mixed signal and circuits, such as wide band RF transmitters, advanced mixed signal integrated systems, optoelectronic RF signal sources, and laser radar systems. | | | |
| ***Title:*** Micro-Technology for Positioning, Navigation, and Timing (Micro PN&T) | 18.201 | 23.396 | 15.000 |
| ***Description:*** The Micro-Technology for Position, Navigation, and Timing (micro-PNT) program is developing low-size, weight, power, and cost (SWaP+C) inertial sensors and timing sources. This suite of sensors, when integrated into an inertial measurement unit (IMU), will enable self-contained navigation and timing in the absence of signals from the Global Positioning System (GPS), due to environmental interference or adversary action such as GPS jamming. The micro-PNT program is developing miniature high performance gyroscopes, accelerometers, and clocks, based on both solid state and | | | |

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| C. Accomplishments/Planned Programs ($ in Millions) | FY 2013 | FY 2014 | FY 2015 |
|---|---|---|---|

atomic technologies. Advanced micro-fabrication techniques under development will enable the fabrication of a single package containing all the necessary devices in a volume the size of a sugar cube. Co-location of atomic physics and MEMS-based devices opens the possibility for utilization of combinatorial algorithms to enable fast start-up time and increased bandwidth of MEMS with the long-term stability and accuracy of MEMS sensors, thus effectively providing very accurate navigation devices in highly dynamic environments. The small SWaP+C of these technologies will enable ubiquitous guidance and navigation on all platforms, including guided munitions, unmanned aerial vehicles (UAVs), and individual soldiers.

The successful realization of micro-PNT depends on the development of new microfabrication processes and novel material systems for fundamentally different sensing modalities, understanding of the error sources at the micro-scale, and understanding of scaling relationships for the size-reduction of sensors based on atomic physics techniques. The micro-PNT program includes research into novel techniques for fabrication and integration of three-dimensional MEMS devices as well as theoretical and experimental studies of new MEMS architectures and geometries for inertial sensing. Atomic physics research includes the development of new geometries and architectures for atomic inertial sensing and the development of techniques for improving the sensitivity and accuracy of miniaturized devices. Advanced research for the program is budgeted in PE 0603739E, Project MT-12.

***FY 2013 Accomplishments:***

- Developed architecture for co-integrated clock, accelerometers, and gyroscope on a single chip with a volume of less than ten cubic millimeters.
- Demonstrated algorithmic techniques for on-chip error correction of an inertial sensor (improving bias stability to 100 parts-per million (ppm)).
- Demonstrated fabrication and functionality of an integrated calibration micro-stage.
- Explored and developed predictive models of error sources for gyroscope and accelerometers.
- Identified physical and algorithmic self-calibration techniques to compensate for stability and drift of inertial sensors, effective to 100 (ppm) scale factor and bias stability.
- Developed design space for chip-scale, atomic navigation sensor.
- Developed hemispherical shell micro-resonators from novel materials (diamond, nickel alloy).
- Developed new fabrication processes for improved packaging and narrow electrode gap alignment.

***FY 2014 Plans:***

- Demonstrate a prototype miniature inertial sensor based on atomic physics.
- Demonstrate laboratory functionality of a MEMS-based IMU with a volume of less than 10mm^3.
- Use predictive error models of gyroscopes and accelerometers to achieve better than 10ppm long term stability of scale factor and bias.

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| C. Accomplishments/Planned Programs ($ in Millions) | FY 2013 | FY 2014 | FY 2015 |
|---|---|---|---|
| - Demonstrate low damping of 3D hemispherical micro-gyroscopes, capable of operating with a high dynamic range in whole angle mode.<br>- Demonstrate on-chip calibration with co-fabricated characterization stages.<br>- Demonstrate improved functionality of Disc Resonant Gyroscope (DRG) with integrated quartz crystal oscillator.<br>***FY 2015 Plans:***<br>- Demonstrate on-chip calibration stages to track bias and scale factor stability repeatable to <100ppm.<br>- Demonstrate a 10mm^3 silica IMU.<br>- Demonstrate a miniaturized, low-drift Nuclear Magnetic Resonance (NMR) gyroscope.<br>- Demonstrate a micro-hemispherical resonant gyroscope, operating in both whole-angle mode and rate mode. | | | |
| ***Title:*** Microscale Plasma Devices (MPD) | 6.138 | 6.300 | 2.000 |
| ***Description:*** The goal of the Microscale Plasma Devices (MPD) program is to design, develop, and characterize MPD technologies, circuits, and substrates. The MPD program will focus on development of fast, small, reliable, high-carrier-density, micro-plasma switches capable of operating in extreme conditions, such as high-radiation and high-temperature environments. Specific focus will be given to methods that provide efficient generation of ions that can perform robust signal processing of radio frequency (RF) through light electromagnetic energy over a range of gas pressures. Applications for such devices are far reaching, including the construction of complete high-frequency plasma-based circuits, and microsystems with superior resistance to radiation and extreme temperature environments. It is envisaged that both two and multi-terminal devices consisting of various architectures will be developed and optimized under the scope of this program. MPDs will be developed in various circuits and substrates to demonstrate the efficacy of different approaches. MPD-based microsystems are demonstrated in DoD applications where electronic systems must survive in extreme environments.<br><br>The MPD applied research program is focused on transferring the fundamental scientific advances funded by PE 0601101E, Project ES-01 to produce complex circuit designs that may be integrated with commercial electronic devices. It is expected that the MPD program will result in the design and modeling tools, as well as the fabrication capabilities necessary to commercially manufacture high-performance microscale-plasma-device-based electronic systems for advanced DoD applications.<br><br>***FY 2013 Accomplishments:***<br>- Verified initial microplasma modeling simulation results against microscale plasma device measurement results to begin optimization of the microplasma modeling-and-simulation design tool (MSDT) for commercial development of microplasma-based electronics.<br>- Investigated the use of microscale plasma devices for protection of sensor systems in extreme environments. | | | |

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| C. Accomplishments/Planned Programs ($ in Millions) | FY 2013 | FY 2014 | FY 2015 |
|---|---|---|---|
| - Completed initial field testing of an MPD-based material for high power electromagnetic applications.<br>***FY 2014 Plans:***<br>- Continue integration of multiple simulation efforts into the modeling-and-simulation design tool (MSDT) for commercial development of microplasma based electronics and DoD systems.<br>- Optimize plasma microcavity materials for DoD systems of interest, demonstrating robustness in high power electromagnetic environments.<br>- Demonstrate and test nonlinear signal processing circuit concepts and architectures based on MPD technologies.<br>***FY 2015 Plans:***<br>- Complete integration of the simulation efforts into the MSDT for commercial development of microplasma based electronics.<br>- Complete final testing of microcavity materials for robustness in a high power electromagnetic application.<br>- Complete demonstration of plasma-based materials and devices for transition to DoD customers. | | | |
| ***Title:*** IntraChip Enhanced Cooling (ICECool)<br><br>***Description:*** The IntraChip Enhanced Cooling (ICECool) program is exploring disruptive technologies that will remove thermal barriers to the operation of military electronic systems, while significantly reducing size, weight, and power consumption. These thermal barriers will be removed by integrating thermal management into the chip, substrate, or package technology. Successful completion of this program will raise chip heat removal rates to above 1 kilowatt/cm^2 and chip package heat removal density to above 1kW/cm^3 in RF arrays and embedded computers.<br><br>Specific areas of focus in this program include overcoming limiting evaporative and diffusive thermal transport mechanisms at the micro/nano scale to provide an order-of-magnitude increase in on-chip heat flux and heat removal density, determining the feasibility of exploiting these mechanisms for intrachip thermal management, characterizing the performance limits and physics-of-failure of high heat density, intrachip cooling technologies, and integrating chip-level thermal management techniques into prototype high power electronics in RF arrays and embedded computing systems.<br><br>***FY 2013 Accomplishments:***<br>- Determined feasibility of implementing advanced thermal management techniques into compact defense electronic systems.<br>- Determined limits of advanced thermal technologies through fundamental studies on intra and interchip cooling.<br>- Initiated efforts to apply intra and interchip cooling as part of the thermal management approach of defense electronic systems.<br>***FY 2014 Plans:***<br>- Prepare and refine initial thermal models of intrachip cooling to explain and predict experimental results.<br>- Demonstrate proof of concept of fundamental building blocks of evaporative intrachip/interchip thermal management including microfabrication in relevant electronic substrates and preliminary thermofluid results. | 11.000 | 21.500 | 20.000 |

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| C. Accomplishments/Planned Programs ($ in Millions) | FY 2013 | FY 2014 | FY 2015 |
|---|---|---|---|
| - Demonstrate application-oriented thermal test vehicles to demonstrate the thermal benefits of embedded microfluidic cooling and model the anticipated electrical performance based on these thermal results.<br>***FY 2015 Plans:***<br>- Demonstrate the full implementation of the fundamental building blocks of evaporative intrachip/interchip cooling in relevant thermal test vehicles.<br>- Demonstrate application-oriented electrical test vehicles to demonstrate the performance benefits of embedded microfluidic cooling and relate these results to system-level performance and size, weight, power and cost (SWaPC) through the use of intrachip thermal management technologies. | | | |
| ***Title:*** In vivo Nanoplatforms (IVN)<br>***Description:*** The In vivo Nanoplatforms (IVN) program seeks to develop the nanoscale systems necessary for in vivo sensing and physiologic monitoring and delivery vehicles for targeted biological therapeutics against chemical and biological (chem-bio) threat agents. The nanoscale components to be developed will enable continuous in vivo monitoring of both small (e.g. glucose, lactate, and urea) and large molecules (e.g. biological threat agents). A reprogrammable therapeutic platform will enable tailored therapeutic delivery to specific areas of the body (e.g. cells, tissue, compartments) in response to traditional, emergent, and engineered threats. The key challenges to developing these systems include safety, toxicity, biocompatibility, sensitivity, response, and targeted delivery. The IVN program will have diagnostic and therapeutic goals that enable a versatile, rapidly adaptable system to provide operational support to the warfighter in any location.<br>***FY 2013 Accomplishments:***<br>- Achieved a safe in vivo nanoplatform sensor to detect one military-relevant analyte (e.g. glucose, nucleic acids) in living cells and/or tissue with a robust signal for greater than one month.<br>- Achieved a safe and effective in vivo nanoplatform therapeutic to reduce a military-relevant pathogen or disease cofactor in living cells by at least 50%.<br>- Facilitated development of a regulatory approval pathway for diagnostic and therapeutic nanoplatforms.<br>***FY 2014 Plans:***<br>- Achieve a safe in vivo nanoplatform sensor to detect two military-relevant analytes (e.g. glucose, nucleic acids) in a small animal with a robust signal for at least six months.<br>- Achieve a safe and effective in vivo nanoplatform therapeutic to reduce a military-relevant pathogen or disease cofactor in a small animal by at least 70%.<br>- Update regulatory approval pathway of identified safe and effective diagnostic and therapeutic nanoplatforms.<br>***FY 2015 Plans:*** | 8.500 | 23.338 | 16.500 |

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| - Achieve a safe in vivo nanoplatform sensor to detect five military-relevant analytes (e.g. glucose, nucleic acids) in a large animal with a robust signal for at least twelve months.<br>- Achieve a safe and effective in vivo nanoplatform therapeutic to reduce a military-relevant pathogen or disease cofactor in a large animal by at least 90%.<br>- Update regulatory approval pathway with results from safety and efficacy testing. | | | |
| ***Title:*** Pixel Network (PIXNET) for Dynamic Visualization | 14.000 | 23.700 | 17.500 |
| ***Description:*** The PIXNET program addresses the squad level capability gap for target detection, recognition and identification in all-weather and day/night missions. The vision of the program is to offer the warfighter a small and versatile infrared (IR) camera that would be affordable for individual soldiers and provide multiple IR band imagery with fusion capability to take full advantage of different wavelength-band phenomenology in a compact single unit. In the future, the availability of the PIXNET camera would enable a peer-to-peer networked system for image sharing within a squad, thereby providing a better common operating picture of the battlefield and significantly enhancing the warfighter's situational understanding. The program aims to develop a low size, weight and power (SWaP), low cost, soldier-portable multiband infrared camera that will provide real-time single and multiple band imagery using thermal and reflected-illumination bands. The camera will also provide fused reflective and thermal band imagery on demand. The use of fused imagery in the PIXNET design will allow the soldier to detect camouflaged targets and distinguish targets from decoys. The PIXNET camera will eliminate limitations posed by current capability, allowing detection, recognition and identification of targets whether in daylight or no-light conditions.<br><br>The PIXNET program will focus on a significant reduction in SWaP and cost of infrared sensor components to enable portability and ability to deploy widely to all participants in the theater. The emphasis on a small form will naturally enable new opportunities such as surveillance with small Unmanned Aerial Vehicles (UAV)s, rifle sights with multiple bands, and vehicle-mounted, helmet-mounted and handheld surveillance systems. The phenomenology of different infrared wavelengths will be exploited. The combination of a smart phone and PIXNET camera at the soldier level will enable more effective tactics, techniques and procedures (TTP) over the current capability. The PIXNET program takes advantage of the computing capability of smart phones to process and fuse multicolor images and send them as videos or still images to the warfighter's helmet-mounted display via a wireless or wired connection. PIXNET capability could be further exploited to enable a fully networked system, such as the Nett Warrior integrated multiple soldier systems capability, with multi-spectral still image and video sharing.<br><br>***FY 2013 Accomplishments:***<br>- Conducted multicolor fusion tests using separate video imagery in visible, shortwave and longwave to determine phenomenological advantages.<br>- Identified several Key Performance Parameters (KPPs) for the brass board design of the PIXNET camera. | | | |

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| - Evaluated four of the KPPs critical to the camera performance: range to identify target, power consumption, weight of hardware, and detector array format.<br>- Completed trade study space and started work in preparation for the System Requirements Review (SRR) for the PIXNET Camera.<br>***FY 2014 Plans:***<br>- Develop and review IR camera design and overall architecture that will demonstrate digital image data transmission and signal processing via wireless connectivity using an android based platform.<br>- Identify parameters required for multicolor helmet-mounted technology for very low SWaP multi-color IR camera.<br>- Complete short wave (SW)/mid-wave (MW) optics design for clip-on weapon sight.<br>- Identify wireless interface protocols for rifles/weapons and helmet displays that are compliant with dismount requirements.<br>- Perform final design of the long-wave IR/very-near IR (LWIR/VNIR) camera cores, optic lens assemblies, display module, image fusion network power components, helmet package, image processing pipeline, and embedded software applications.<br>- Demonstration of brass board components for the LWIR/VNIR helmet camera.<br>***FY 2015 Plans:***<br>- Refine algorithms to fuse data from thermal and reflective bands with good image registration.<br>- Complete interim small form-factor camera integration and demonstrate connectivity to heads-up display and Android-based platform.<br>- Readout Integrated Circuit (ROIC) tapeout and SW/MW fabrication.<br>- Complete fabrication of LWIR/VNIR and start final integration of helmet camera.<br>- Demonstrate multicolor image acquisition by interim PIXNET camera, data transmission to Android platform, image fusion by Android platform, and viewing of fused imagery on heads-up display. | | | |
| ***Title:*** Arrays at Commercial Timescales (ACT)<br>***Description:*** Phased arrays are critical system components for high performance military electronics with widespread applications in communications, electronic warfare and radar. The DoD relies heavily on phased arrays to maintain technological superiority in nearly every theater of conflict. The DoD cannot update these high cost specialized arrays at the pace necessary to effectively counter adversarial threats under development using commercial-of-the-shelf components that can undergo technology refresh far more frequently. The Arrays at Commercial Timescales (ACT) program will develop adaptive and standardized digital-at-every-element arrays. The hand designed, static analog beamformers will be replaced with cost effective digital array systems capable of a yearly technology refresh. By doing so, phased arrays will become ubiquitous throughout the DoD, moving onto many platforms for which phased arrays had been previously prohibitively expensive to develop or maintain. The basic research component of this program is budgeted under PE 0601101E, Project ES-01. | - | 23.856 | 25.000 |

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| ***FY 2014 Plans:***<br>- Initiate development of common hardware components for phased-array elements that can be seamlessly integrated into a wide range of platforms and implement the first iteration of the common components in a state-of-the-art fabrication process.<br>- Initiate the development of digital array systems with performance capabilities that evolve with Moore's law at commercial time scales.<br>- Initiate the development of electromagnetic (EM) interface elements capable of reconfiguring for various array use cases and operational specifications.<br>- Demonstrate reconfigurability of EM interface components for various array performance specifications and demonstrate compatibility with common digital back-end.<br>- Identify government application spaces and transition paths that will make use of ACT common modules and reconfigurable antenna apertures.<br>***FY 2015 Plans:***<br>- Continue development of common hardware components for phased-array elements that can be seamlessly integrated into a wide range of platforms and implement the second iteration of the common components in a state-of-the-art fabrication process and test functionality in a laboratory environment.<br>- Demonstrate Common Module hardware viability through government testing of delivered hardware components in a government furnished system platform.<br>- Continue the development of EM interface elements capable of reconfiguring for various array use cases and operational specifications, and demonstrate tuning over an octave of bandwidth and over multiple polarization settings.<br>- Continue to demonstrate reconfigurability of EM interface components for various array performance specifications, and demonstrate compatibility with common digital back-end.<br>- Continue to identify government application spaces and transition paths for the ACT Common Module and reconfigurable antenna apertures. | | | |
| ***Title:*** Micro-coolers for Focal Plane Arrays (MC-FPA)<br><br>***Description:*** The Micro-coolers for Focal Plane Arrays (MC-FPA) program will develop low Size, Weight, Power, and Cost (SWaP-C) cryogenic coolers for application in high performance IR cameras. The sensitivity of an IR focal-plane array (FPA) is improved by cooling its detectors to cryogenic temperatures. The disadvantages of state-of-the-art Stirling cryo-coolers used for high performance IR FPAs are large size, high power and high cost. On the other hand, thermoelectric (TE) coolers used in low performance IR cameras are relatively small, high power, and it is difficult to achieve temperatures below 200 Kelvin (K).<br><br>To reduce IR camera SWaP-C, innovations in cooler technology are needed. This program will exploit the Joule-Thomson (J-T) cooling principle, in a silicon-based MEMS technology, for making IR FPA coolers with very low SWaP-C. MEMS microfluidics, | - | 5.000 | 1.500 |

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| piezoelectric MEMS, and complementary metal-oxide semiconductor (CMOS) electronics will be used to demonstrate an integrated cold head and compressor, all in a semiconductor chip. Since a J-T cooler works by cooling from gas expansion, the coefficient of performance is expected to be much higher than state-of-the-art TE coolers, while being significantly smaller than Stirling coolers. The chip-scale J-T cooler will be designed for pressure ratios of 4 or 5 to 1 with high compressor frequency in a small volume. The goal of the MC-FPA program will be to demonstrate cooling down to 150 K. The chip-scale micro-coolers will cost less and will be significantly smaller than current Stirling coolers. Once the proof-of-principle is demonstrated, the subsequent program effort will focus on transitioning to chip-scale manufacture on 8-12 inch wafers, resulting in cooler costs decreasing to as low as $50. An extended wavelength-range short-wave IR detector will be integrated with a micro-cooler for demonstration of the MC-FPA. The basic research component of this program is budgeted under PE 0601101E, Project ES-01.<br><br>***FY 2014 Plans:***<br>- Develop detector design for response in 1-2.4 microns.<br>- Perform materials growth and characterization for detector fabrication.<br>- Process Cadmium Zinc Telluride (CdZnTe) substrates for epitaxy.<br>- Complete initial analysis to determine input cell design for readout integrated circuit (ROIC).<br>- Fabricate and test a single stage MC-FPA.<br>- Develop 640X480 extended shortwave infrared (1-2.4 micrometer cutoff) FPA.<br>- Design a readout integrated circuit (ROIC) for the IR FPA chip.<br>- Demonstrate camera electronics for the FPA with provision for chip-scale micro-cooler.<br><br>***FY 2015 Plans:***<br>- Fabricate 3-stage J-T micro-cooler.<br>- Hybridize FPA to ROIC and integrate 3-stage J-T micro-cooler with complete backend packaging.<br>- Complete camera integration & housing.<br>- Complete camera tests and demo. | | | |
| ***Title:*** Vanishing Programmable Resources (VAPR)<br><br>***Description:*** The Vanishing Programmable Resources (VAPR) program will create electronic systems capable of physically disappearing (either in whole or in part) in a controlled, triggerable manner. The program will develop and establish an initial set of materials and components along with integration and manufacturing capabilities to undergird a fundamentally new class of electronics defined by their performance and transience. These transient electronics ideally should perform in a manner comparable to Commercial Off-The-Shelf (COTS) systems, but with limited device persistence that can be programmed, adjusted in real-time, triggered, and/or sensitive to the deployment environment. Applications include sensors for conventional indoor/ outdoor environments (buildings, transportation, materiel), environmental monitoring over large areas, and simplified diagnosis, treatment, and health monitoring in the field. VAPR will build out an initial capability to make transient electronics a deployable | - | 9.645 | 5.500 |

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| technology for the DoD and Nation. The technological capability developed through VAPR will be demonstrated through a final test vehicle of a transient beacon. Basic research for the VAPR program is being performed in PE 0601101E, Project TRS-01.<br><br>To manufacture transient systems at scale will require significant research and development into: higher levels of circuit integration and complexity to realize advanced circuit functionalities; integrated system designs to achieve required function (in modes that offer programmed or triggered transience); integration of novel materials into circuit fabrication processes; and development of new packaging strategies. The efficacy of the technological capability developed through VAPR will be demonstrated through a final test vehicle of a transient sensor system. The goal is to develop a suite of design principles, develop strategies and pathways, process flows, tools and basic components that are readily generalizable and can be leveraged towards the development of many other transient electronics devices.<br><br>***FY 2014 Plans:***<br>- Begin developing foundry fabrication of transient electronics with key functions (RF, memory, digital logic, power supply, etc.).<br>- Begin developing increased circuit integration and complexity to implement advanced functionalities.<br>- Initiate transient sensors and power supply strategy development.<br>- Begin developing transient device fabrication approaches.<br>- Initiate transience mode demonstration in test vehicles.<br>***FY 2015 Plans:***<br>- Achieve a transience time of less than or equal to 5 minutes for simple electronic devices.<br>- Reduce the variability of transience time to less than or equal to 90 seconds for simple electronic devices.<br>- Demonstrate capability to have reliable operation of simple transient electronic devices for greater than 24 hours after deployment, with subsequent controlled transience. | | | |
| ***Title:*** Gargoyle<br><br>***Description:*** Sensors, processors and users transmit data on a massive scale; however processing capabilities cannot keep pace. The result is missed warnings and delayed reaction. Digital electronics, while indispensable, cannot scale with the unprecedented demand for high-throughput processing. For example, aggregate communications through optical fibers are currently >100 Terabit/sec (Tbps) worldwide and are expected to exceed 1 Petabit/sec by 2020. In these high-rate optical links, signatures of malware propagation or denial of service attacks become small needles in a very large haystack. Conventional digital processing attempts to extract relevant information, but it is not nearly fast enough to keep up, and falls far short of 100% aperture capture.<br><br>Gargoyle will develop photonic correlators for critical data processing tasks to provide near-zero latency, high-throughput processing of both digital and analog data. Advanced optical correlator technology has the potential to scale up with ever- | - | - | 2.000 |

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| increasing bit rates. Applications for this technology include direct sequence spread spectrum bandwidths exceeding 10 Gigahertz (GHz), and cyber defense in fiber-optic networks with scalability to future transmission rates exceeding 10 Tbps.<br><br>***FY 2015 Plans:***<br>- Simulate photonic components for fundamental data-processing tasks, such as high-rate Fourier and Hilbert transforms, and cross-correlation.<br>- Simulate, design and test processing pipelines for dispreading of Direct Sequence Spread Spectrum (DSSS) RF communications.<br>- Design a broadband wireless communication DSSS link consisting of transmitter and receiver with spreading/dispreading factors exceeding 1,000. | | | |
| ***Title:*** Cold-Atom Microsystems (CAMS) | - | - | 4.000 |
| ***Description:*** Precision measurements based on atomic physics principles are the underlying technology of the most accurate measurement devices in the world, including practical devices such as atomic clocks and inertial sensors, as well as laboratory tests of fundamental physics. The field of atomic physics was revolutionized in the 1980's with the development of the technique of laser cooling of atoms. Utilizing precisely tuned lasers with high spectral purity (narrow linewidth), atoms may be cooled down to nearly absolute zero temperature. So-called cold atoms are of great practical value to DoD position, navigation, and timing (PNT) systems, for two reasons. First, because the atoms are nearly unmoving, it is possible to make relatively long-duration measurements of their internal state, with minimal collisions between atoms or between atoms and the walls of the containing vessel. This has led to the development of high-performance laboratory-based cold-atom fountain clocks, such as the U.S. national time standard, NIST-F1, and the rubidium fountains that underpin the U. S. Naval Observatory master clock. Secondly, taking advantage of the relatively slow velocities of cold atoms, atomic interferometers have been demonstrated, which provide the highest precision measurements of rotation and acceleration. Under the DARPA micro-PNT program, miniature high-performance cold atom-based atomic clocks, gyroscopes, and accelerometers are being developed and have demonstrated superior performance in relatively low size, weight, and power (SWaP).<br><br>The Cold-Atom Microsystems (CAMS) program will develop enabling component technologies to support the practical deployment of cold-atom based microsystems, including low-SWaP atomic clocks, gyroscopes, and accelerometers. Technologies under investigation include high-efficiency narrow-linewidth laser sources, high-efficiency optical modulators, miniature high-isolation optical switches, compact low-loss optical isolators, miniature systems for laser frequency locking and agile frequency control, miniature ultra-high vacuum chambers and vacuum pumps, and techniques for controlling the vapor pressure of alkali metal atomic species over the DoD operating temperature range.<br><br>***FY 2015 Plans:*** | | | |

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| - Demonstrate miniature low-loss optical isolators.<br>- Develop novel high-efficiency narrow-linewidth laser architectures.<br>- Demonstrate alkali vapor pressure control over the DoD operating temperature range.<br>- Develop and test of microscale high isolation (> 80 dB) optical shutters.<br>- Develop microscale vacuum pumps capable of sustaining vacuum pressure of 1e-8 Torr. | | | |
| ***Title:*** Direct SAMpling Digital ReceivER (DISARMER) | - | 2.000 | 2.000 |
| ***Description:*** The goal of the Direct SAMpling Digital ReceivER (DISARMER) program is to produce a hybrid photonic-electronic analog-to-digital converter (ADC) capable of directly sampling the entire X-band (8-12 Gigahertz (GHz)). Conventional electronic wideband receivers are limited in dynamic range by both the electronic mixer and the back-end digitizers. By employing an ultra-stable optical clock, the DISARMER program will allow for mixer-less digitization and thereby improve the dynamic range 100x over the state of the art. Such a wide bandwidth, high fidelity receiver will have applications in electronic warfare and signals intelligence systems while dramatically reducing the cost, size and weight of these systems.<br><br>The DISARMER program will develop a low jitter mode-locked laser to be used as the sampling source. The program will also develop a novel photonic processor chip on a silicon platform capable of hybrid electronic-photonic track-and-hold functionality and coherent photo-detection. These silicon photonic integrated circuits will be integrated with CMOS driver circuits and packaged for integration in the full DISARMER system. This program has advanced technology development efforts funded in PE 0603739E, Project MT-15.<br><br>***FY 2014 Plans:***<br>- Complete preliminary design of photonic processor chip.<br>- Complete preliminary design of low jitter mode-locked laser with 8 GHz repetition rate.<br>***FY 2015 Plans:***<br>- Complete architecture evaluation to determine the best mix of electronics and photonics for optimized performance and power consumption.<br>- Fabricate and test the building blocks of the photonic processor.<br>- Package photonic processor chip and electronic integrated circuit chip.<br>- Demonstrate and test mode locked laser with 8 GHz repetition rate, 1 ps pulse width, and 5 fs of integrated timing jitter. | | | |
| ***Title:*** Fast and Big Mixed-Signal Designs (FAB) | - | - | 4.000 |
| ***Description:*** Developing capabilities to intermix and tightly integrate silicon processes which are currently supported at different scaling nodes and by different vendors is critical to increasing the capabilities of high-performance military microelectronics. Specifically, silicon-germanium (SiGe) processes allow complementary metal-oxide semiconductor (CMOS) logic to be integrated | | | |

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| with RF heterojunction bipolar transistors (HBTs), which enables mixed-signal circuits having RF analog capabilities tightly coupled to digital processing. The Fast and Big Mixed-Signal Designs (FAB) program proposes to engage with a semiconductor fabrication partner to develop a SiGe fabrication process integrating 14nm CMOS. The SiGe technology will enable the development of faster, more precise RF and signal acquisition components, while the 14nm CMOS process will enable low-power digital circuitry that can provide the large throughput required for data from the analog components. The ability to mix massive digital computation at lower power with the fast sampling enabled by Silicone Germanium (SiGe) HBTs gives a powerful platform for future generations of Electronic Warfare (EW) systems. This program will seek to overcome the tradeoffs in providing the highest performance analog performance versus the densest and lowest power digital processes. Success will enable higher performance, lower cost, and more rapid insertion of advanced process technology into military electronics.<br><br>***FY 2015 Plans:***<br>- Determine the best choices for the RF and digital technologies and the best methods of co-integration (monolithic, through-silicon via (TSV)s, interposer, etc.) in order to achieve program objectives, along with identifying partner(s) for fabrication and/or integration.<br>- Begin circuit design activities to determine performance benefits of new processes enabled by the program.<br>- Study the best technology for various RF functional blocks for optimal use of mixed technologies. | | | |
| ***Title:*** Microscale Power Conversion (MPC) | 8.561 | 8.800 | - |
| ***Description:*** Today's power amplifiers utilize large, bulky, independently designed fixed voltage power supplies that fundamentally limit Radio Frequency (RF) system output power, power efficiency and potential for integration. The Microscale Power Conversion (MPC) program is developing X-band RF transmitters as system-in-package modules, in which integrated circuit power amplifiers are integrated with dynamic, variable voltage power supplies using high-speed power switches. Such an integrated microsystem will support military applications requiring several hundred Megahertz (MHz) of RF envelope bandwidth at large peak-to-average power ratios. This integration approach will realize RF systems with significantly higher overall power efficiency and waveform diversity by changing from a fixed power supply architecture to a dynamic power supply architecture. The program is structured in two technical tracks. The first track is developing high-speed power switch technology to be used in the design of dynamic power supply and modulator circuits. The second track is developing the simultaneous co-design and integration of the RF power amplifier and dynamic power supply circuits to achieve maximum overall power efficiency for the desired waveforms of interest. The impact of this program will be the increased deployment of MPC RF transmitter systems on DoD platforms due to their more compact size, high efficiency, lower lifecycle cost and enhanced RF performance enabling, for example, significantly communications rates.<br><br>***FY 2013 Accomplishments:*** | | | |

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| - Continued development of very high frequency, low-loss power switch technology for implementing large envelope-bandwidth modulators for RF power amplifiers.<br>- Initiated co-designs of advanced X-band power amplifier technologies to include drain and gate bias modulation, dynamic output impedance matching, and closed-loop control.<br>- Demonstrated second generation power supply modulator with high efficiency in a laboratory environment.<br>- Designed and prototyped second generation transmitter architectures for highly efficient handling of large peak-to-average ratio RF waveforms for military systems.<br>- Fabricated low-loss packages and monolithically integrated switches for amplifier-modulator circuits.<br>***FY 2014 Plans:***<br>- Complete very high frequency, low-loss power switch technology for implementing large envelope-bandwidth modulators for RF power amplifiers.<br>- Demonstrate final co-designs of advanced X-band transmitter to include drain and gate bias modulation, dynamic output impedance matching, and closed-loop control with fast-switching power modulation.<br>- Furnish power switch process design kits to DoD contractors for use in future power supply modulator or power amplifier designs.<br>- Demonstrate RF transmission of relevant military waveforms for electronic warfare applications. | | | |
| ***Title:*** Photonically Optimized Embedded Microprocessor (POEM)<br>***Description:*** Based upon current scaling trends, microprocessor performance is projected to fall far short of future military needs. Microprocessor performance is saturating and leading to reduced computational efficiency because of the limitations of electrical communications. The POEM program will demonstrate chip-scale, silicon-photonic technologies that can be integrated within embedded microprocessors for seamless, energy-efficient, high-capacity communications within and between the microprocessor and dynamic random access memory (DRAM). This technology will propel microprocessors onto a higher performance trajectory by overcoming this "memory wall".<br>***FY 2013 Accomplishments:***<br>- Demonstrated a photonic link between two chips fabricated in a DRAM foundry consuming 2.8 picojoules (pJ/bit) including control and driver circuitry.<br>- Continued to develop and improve complementary metal-oxide semiconductor (CMOS)-compatible modulator, multiplexer, coupler, and photodetector devices and associated drivers for low-power, high capacity photonic links for insertion in final demonstration.<br>- Demonstrated a complete, integrated 8-channel photonic transmitter operating at 100 Gigabit/s and 330 femtojoules per bit (fJ/bit), and a complete, integrated, 8-channel photonic receiver operating at 80 Gb/s and 500 fJ/bit.<br>- Developed an on-chip, uncooled, frequency-stabilized laser operating at ~7% wall plug efficiency. | 15.000 | 1.500 | - |

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|---|---|---|---|
| - Identified applications where a cluster of photonically optimized microprocessors is useful and designed the cluster architecture, photonic network, and parallel algorithms for community analysis on large graphs.<br><br>***FY 2014 Plans:***<br>- Demonstrate a photonic link between a CMOS chip and a DRAM chip consuming low (few picojoule (pJ)) energy/bit employing foundry-compatible photonic devices and respective control and driver circuits.<br>- Fabricate and test optical receiver circuits with 200 nanoseconds (ns) locking time and consuming 10 pJ/bit.<br>- Design and test new algorithms that effectively parallelize graph analytic problems, taking advantage of the high bandwidth photonic interconnects.<br>- Study and optimize the material stack for fabricating an on-chip, uncooled laser operating at 1550 nm and ~ 10% wall plug efficiency. | | | |
| ***Title:*** Advanced X-Ray Integrated Sources (AXIS)<br><br>***Description:*** The Advanced X-Ray Integrated Sources (AXIS) program developed tunable, mono-energetic, spatially coherent X-ray sources with greatly reduced size, weight and power while dramatically increasing their electrical efficiency through application of micro-scale engineering technologies such as MEMS and NEMS. Such X-ray sources enabled new versatile imaging modalities based on phase contrast techniques which are 1000X more sensitive than the conventional absorption contrast imaging. Such imaging modalities enabled design verification of integrated circuits to validate trustworthiness as well as Forward Surgical Team imaging of soft tissues and vascular injuries from blunt trauma without the injection of a contrast enhancing agent. The radiation dose required for imaging will also be reduced.<br><br>The Applied Research component of this effort focused on applying basic research discoveries to the development of a compact, pulsed X-ray source. Such sources are a necessary component to enable future technologies with high-speed motion tomographic imaging capabilities and the design verification of integrated circuits. This program also included related basic research efforts funded under PE 0601101E, Project ES-01.<br><br>***FY 2013 Accomplishments:***<br>- Fabricated and demonstrated a short-lifetime photoconductor switched tip-on-post (Spindt) field emitter with short pulse duration, high pulse repetition rate, and low emittance.<br>- Began fabrication of an advanced hard X-ray source based on a whispering gallery mode resonator with multi-layer reflectivity for confinement and gain.<br>- Coordinated the development of devices capable of producing synchrotron-quality X-rays by integrating the most successful components (cathodes, accelerators, undulators & lasers) in the program. | 8.000 | - | - |

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| C. Accomplishments/Planned Programs ($ in Millions) | FY 2013 | FY 2014 | FY 2015 |
|---|---|---|---|
| - Obtained X-ray images from an array of micro-focused X-ray sources fabricated for the AXiS program. | | | |
| ***Title:*** Quantum Information Science (QIS)<br><br>***Description:*** The Quantum Information Science (QIS) program explored all facets of the research necessary to create new technologies based on quantum information science. Research in this area has the ultimate goal of demonstrating the potentially significant advantages of uniquely quantum effects in communication and computing. The QIS program addressed the fundamental material science and physics associated with uniquely quantum effects in materials. The primary technical challenges include loss of information due to quantum decoherence and the practical limitations associated with operation temperatures, susceptibility to electronic and magnetic noise, coupling between quantum devices, etc. Theoretical efforts in QIS investigated novel techniques for preserving coherence, distributing quantum entanglement, and efficiently modeling quantum operations. Complementary experiments sought to demonstrate quantum devices with better coherence properties than existing devices and to implement entangling operations between two or more quantum devices. Future technologies utilizing quantum information science could enable ultra-secure communications; faster algorithms for optimization and simulation in logistics, war gaming, and pharmaceutical development; and new methods for image and signal processing in measurement and signature intelligence activities (MASINT).<br><br>***FY 2013 Accomplishments:***<br>- Improved speed and accuracy of numerical modeling of quantum device operation.<br>- Developed design, growth, and fabrication techniques for enhancement-mode quantum devices with improved performance.<br>- Demonstrated coupling of a spin qubit to a superconducting resonator for transport of quantum information over centimeter-scale distances. | 1.138 | - | - |
| ***Title:*** Systems of Neuromorphic Adaptive Plastic Scalable Electronics (SyNAPSE)<br><br>***Description:*** The vision of the Systems of Neuromorphic Adaptive Plastic Scalable Electronics (SyNAPSE) program was the development of biological-scale neuromorphic electronic systems for autonomous, unmanned, robotic systems where humans are currently the only viable option. Successful development of this technology could revolutionize warfare by providing intelligent terrestrial, underwater, and airborne systems that remove humans from dangerous environments and remove the limitations associated with today's remote-controlled robotic systems. Applications for neuromorphic electronics include not only robotic systems, but also natural human-machine interfaces and diverse sensory and information integration applications in the defense and civilian sectors.<br><br>***FY 2013 Accomplishments:***<br>- Fabricated neuromorphic chips of 1 million neurons performing behavioral tests in the virtual environment. | 6.842 | - | - |

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| C. Accomplishments/Planned Programs ($ in Millions) | FY 2013 | FY 2014 | FY 2015 |
|---|---|---|---|
| - Demonstrated functionality of chip performing perception challenge task and benchmark against state-of-the-art algorithms and methods.<br>- Determined scalability of hardware systems and future densities and power consumption for next-generation systems. | | | |
| ***Title:*** Self-HEALing mixed-signal Integrated Circuits (HEALICs)<br><br>***Description:*** Virtually all DoD systems employ mixed-signal circuits for functions such as communications, radar, navigation, sensing, and high-speed image and video processing. A self-healing integrated circuit is defined as a design that is able to sense undesired circuit/system behaviors and correct them automatically. As semiconductor process technologies are being scaled to even smaller transistor dimensions, there is a dramatic increase in intra-wafer and intra-die process variations, which has a direct impact on yield and realized circuit performance, including significantly increased sensitivity to temperature and aging effects. The Self-HEALing mixed-signal Integrated Circuits (HEALICs) program developed technologies to autonomously maximize the number of fully operational mixed-signal systems-on-a-chip (SoC) per wafer that meet all performance goals in the presence of extreme process technology variations, and to sustain circuit performance in the field in the face of changing environmental conditions and component aging.<br><br>This applied research program developed techniques to regain lost performance and stabilize operation of mixed-signal SoCs over system lifetimes. Consequently, the long-term reliability and performance of DoD electronic systems may be enhanced.<br><br>***FY 2013 Accomplishments:***<br>- Continued to integrate previously demonstrated mixed-signal circuit designs into full self-healing microsystems/SoCs and showed self-healing techniques capable of achieving >95% performance yield with <5% power consumption overhead.<br>- Continued to develop global self-healing control at the microsystem/SoC level.<br>- Demonstrated self-healing design strategies to compensate for chip aging.<br>- Made design data for self-healing circuit library widely available for DoD user access. | 1.940 | - | - |
| ***Title:*** Efficient Linearized All-Silicon Transmitter ICs (ELASTx)<br><br>***Description:*** The Efficient Linearized All-Silicon Transmitter ICs (ELASTx) program developed revolutionary high-power/high-efficiency/high-linearity single-chip millimeter (mm)-wave transmitter integrated circuits (ICs) in leading-edge silicon technologies for future miniaturized communications and sensor systems on mobile platforms. The high levels of integration possible in silicon technologies enable on-chip linearization, complex waveform synthesis, and digital calibration and correction. Military applications include ultra-miniaturized transceivers for satellite communications-on-the-move, collision avoidance radars for micro-/nano-air vehicles, and ultra-miniature seekers for small munitions. The technology developed under this program was leveraged to improve the performance of high-power amplifiers based on other non-silicon technologies, through heterogeneous integration strategies. Significant technical obstacles were overcome including the development of highly efficient circuits for increasing | 7.622 | - | - |

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| C. Accomplishments/Planned Programs ($ in Millions) | FY 2013 | FY 2014 | FY 2015 |
|---|---|---|---|
| achievable output power of silicon devices (e.g., device stacking, power combining) at mm-waves; scaling high-efficiency amplifier classes to the mm-wave regime; integrated linearization architectures for complex modulated waveforms; and robust RF/mixed-signal isolation strategies.<br><br>***FY 2013 Accomplishments:***<br>- Demonstrated watt-level, high power-added efficiency (PAE) silicon-based PA circuits at W-band frequencies.<br>- Demonstrated linearized transmitter circuits based on high-PAE power amplifiers (Pas) at W-band frequencies with complex modulated waveforms.<br>- Demonstrated fully-integrated, watt-level, System-on-Chip transmitter at W-band frequencies with complex modulated waveforms.<br>- Initiated development of watt-level, high PAE silicon-based PA circuits at D-band frequencies.<br>- Initiated development of linearized transmitter circuits based on high PAE PAs at D-band frequencies with complex modulated waveforms. | | | |
| ***Title:*** Analog-to-Information (A-to-I) Look-Through | 2.800 | - | - |
| ***Description:*** The Analog-to-Information (A-to-I) Look-Through program fundamentally improved the operational bandwidth, linearity, and efficiency of electronic systems where the objective is to receive and transmit information using electromagnetic (radio) waves under extreme size/weight/power and environmental conditions required for DoD applications. The A-to-I Look-Through program developed ultra-wideband digital radio frequency (RF) receivers based on Analog-to-Information Converter (AIC) technology. Compared to conventional RF receivers, AIC-based designs increased receiver dynamic range and frequency band of regard while reducing data glut, power consumption and size. Likewise, limitations of current-art power amplifier technology in simultaneously achieving high operational bandwidth, linearity, efficiency and power has resulted in well documented instances of electronic fratricide. This program overcomes these limitations by converting digital signals directly to high power RF analog signals, thus eliminating the traditional high power amplifiers that are limited by the above-mentioned tradeoffs. Transition is anticipated into airborne SIGINT and electronic warfare systems, as well as ground-based special operations forces systems.<br><br>***FY 2013 Accomplishments:***<br>- Finalized technology transition plans and transitioned A-to-I receivers to operationally-focused end user organizations.<br>- Completed design, tape out, fabrication and characterization in laboratory environment of 16-tap Look-Through transmitters with high linearity, high power, wide bandwidth and high efficiency.<br>- Demonstrated capability of transmitter cells and associated distributed architectures to be re-programmed to perform distributed receiver-mode functions in order to mitigate electronic fratricide. | | | |

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| C. Accomplishments/Planned Programs ($ in Millions) | FY 2013 | FY 2014 | FY 2015 |
|---|---|---|---|
| - Demonstrated the transmitter performance in representative environments for a DoD system of interest achieving a 60 dB performance.<br>- Initiated design and tape out of final, large-scale Look-Through transmitters meeting the final program goals of high linearity, high power, wide bandwidth and high efficiency.<br>- Initiated planning for laboratory testing of final, large-scale Look-Through transmitters, demonstrating the final transmitter performance in realistic environments for a DoD system of interest. | | | |
| ***Title:*** Advanced Wide FOV Architectures for Image Reconstruction & Exploitation (AWARE)<br><br>***Description:*** The Advanced Wide Field of View (FOV) Architectures for Image Reconstruction & Exploitation (AWARE) program addressed the passive imaging needs for multi-band, wide-field-of-view (FOV) and high-resolution imaging for ground and near-ground platforms. The AWARE program solved the technological barriers that will enable wide-FOV, high resolution and multi-band camera architectures by focusing on four major tasks: high space-bandwidth product (SBP) camera architecture; small-pitch-pixel focal plane array architecture; broadband focal plane array architecture; and multi-band focal plane array architecture.<br><br>The AWARE program demonstrated technologies such as detectors, focal plane arrays, read-out integrated circuitry, and computational imaging that enable wide FOV and high space-bandwidth, novel optical designs, high resolution and multiple wavelength-band imagers. These technologies will be integrated into subsystem demonstrations under the related project in PE 0603739E, MT-15.<br><br>***FY 2013 Accomplishments:***<br>- Demonstrated a 2 gigapixel camera with greater than 100 degree FOV.<br>- Continued development of a 10 gigapixel camera.<br>- Completed AWARE-2 camera with glass microcameras and demonstrated 2-gigapixel video. AWARE-2 will have 38.4 milliradian (mrad) instantaneous (I)FOV, 100 degrees by 60 degrees FOV, 2 gigapixels, and entrance pupil 11.1 mm.<br>- Completed AWARE-10 camera with 10-Gigapixel and 12.6 mrad IFOV.<br>- Completed field tests for both cameras. | 6.000 | - | - |
| **Accomplishments/Planned Programs Subtotals** | 192.349 | 233.469 | 179.203 |

**D. Other Program Funding Summary ($ in Millions)**

N/A

**Remarks**

**E. Acquisition Strategy**

N/A

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**F. Performance Metrics**

Specific programmatic performance metrics are listed above in the program accomplishments and plans section.