| Exhibit R-2, RDT&E Budget Item Justification: PB 2013 Defense Advanced Research Projects Agency | DATE: February 2012 |
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| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 3: *Advanced Technology Development (ATD)* | R-1 ITEM NOMENCLATURE<br>PE 0603739E: *ADVANCED ELECTRONICS TECHNOLOGIES* |

| COST ($ in Millions) | FY 2011 | FY 2012 | FY 2013 Base | FY 2013 OCO | FY 2013 Total | FY 2014 | FY 2015 | FY 2016 | FY 2017 | Cost To Complete | Total Cost |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Total Program Element | 181.118 | 150.286 | 111.008 | - | 111.008 | 104.665 | 101.412 | 95.412 | 88.843 | Continuing | Continuing |
| MT-12: *MEMS AND INTEGRATED MICROSYSTEMS TECHNOLOGY* | 77.179 | 62.053 | 36.466 | - | 36.466 | 43.188 | 29.642 | 37.642 | 32.095 | Continuing | Continuing |
| MT-15: *MIXED TECHNOLOGY INTEGRATION* | 103.939 | 88.233 | 74.542 | - | 74.542 | 61.477 | 71.770 | 57.770 | 56.748 | Continuing | Continuing |

**A. Mission Description and Budget Item Justification**

The Advanced Electronics Technology program element is budgeted in the Advanced Technology Development Budget Activity because it seeks to design and demonstrate state-of-the-art manufacturing and processing technologies for the production of various electronics and microelectronic devices, sensor systems, actuators and gear drives that have military applications and potential commercial utility. Introduction of advanced product design capability and flexible, scalable manufacturing techniques will enable the commercial sector to rapidly and cost-effectively satisfy military requirements.

The MicroElectroMechanical Systems (MEMS) and Integrated Microsystems Technology project is a broad, cross-disciplinary initiative to merge computation and power generation with sensing and actuation to realize a new technology for both perceiving and controlling weapons systems and battlefield environments. MEMS applies the advantages of miniaturization, multiple components and integrated microelectronics to the design and construction of integrated electromechanical and electro-chemical-mechanical systems to address issues ranging from the scaling of devices and physical forces to new organization and control strategies for distributed, high-density arrays of sensor and actuator elements. The project will also address thermal management, navigation and positioning technology challenges.

The goal of the Mixed Technology Integration project is to leverage advanced microelectronics manufacturing infrastructure and DARPA component technologies developed in other projects to produce mixed-technology microsystems. These 'wristwatch size', low-cost, lightweight and low power microsystems will improve the battlefield awareness and security of the warfighter and the operational performance of military platforms. The chip assembly and packaging processes currently in use produce a high cost, high power, large volume and lower performance system. This program is focused on the monolithic integration of mixed technologies to form batch-fabricated, mixed technology microsystems 'on-a-single-chip' or an integrated and interconnected 'stack-of-chips'. The ability to integrate mixed technologies onto a single substrate will increase performance and reliability, while driving down size, weight, volume and cost.

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| B. Program Change Summary ($ in Millions) | FY 2011 | FY 2012 | FY 2013 Base | FY 2013 OCO | FY 2013 Total |
|---|---|---|---|---|---|
| Previous President's Budget | 197.098 | 160.286 | 111.499 | - | 111.499 |
| Current President's Budget | 181.118 | 150.286 | 111.008 | - | 111.008 |
| Total Adjustments | -15.980 | -10.000 | -0.491 | - | -0.491 |
| • Congressional General Reductions | -1.002 | - | | | |
| • Congressional Directed Reductions | - | -10.000 | | | |
| • Congressional Rescissions | -2.586 | - | | | |
| • Congressional Adds | - | - | | | |
| • Congressional Directed Transfers | - | - | | | |
| • Reprogrammings | -7.319 | - | | | |
| • SBIR/STTR Transfer | -5.073 | - | | | |
| • TotalOtherAdjustments | - | - | -0.491 | - | -0.491 |

**Change Summary Explanation**

FY 2011: Decrease reflects reductions for the Section 8117 Economic Adjustment, internal below threshold reprogrammings, rescissions and the SBIR/STTR transfer.

FY2012: Decrease reflects reduction to new starts.

FY 2013: Decrease reflects minor repricing.

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| COST ($ in Millions) | FY 2011 | FY 2012 | FY 2013 Base | FY 2013 OCO | FY 2013 Total | FY 2014 | FY 2015 | FY 2016 | FY 2017 | Cost To Complete | Total Cost |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MT-12: *MEMS AND INTEGRATED MICROSYSTEMS TECHNOLOGY* | 77.179 | 62.053 | 36.466 | - | 36.466 | 43.188 | 29.642 | 37.642 | 32.095 | Continuing | Continuing |

**A. Mission Description and Budget Item Justification**

The MicroElectroMechanical Systems (MEMS) and Integrated Microsystems Technology program is a broad, cross-disciplinary initiative to merge computation and power generation with sensing and actuation to realize a new technology for both perceiving and controlling weapons systems and battlefield environments. Using fabrication processes and materials similar to those used to make microelectronic devices, MEMS applies the advantages of miniaturization, multiple components and integrated microelectronics to the design and construction of integrated electromechanical and electro-chemical-mechanical systems. The MEMS program addresses issues ranging from the scaling of devices and physical forces to new organization and control strategies for distributed, high-density arrays of sensor and actuator elements. These issues include microscale power and actuation systems as well as microscale components that survive harsh environments. The microfluidic molecular systems effort will develop automated microsystems that integrate biochemical fluid handling capability along with electronics, optoelectronics and chip-based reaction and detection modules for tailored sequence analysis to monitor environmental conditions, health hazards and physiological states. Thermal management technologies will develop heat resistant thermal layers to provide efficient operation for cooling electronic devices. Another focus in micro technologies is to improve navigation, position and timing capabilities for uncompromised navigation and positioning in today's dynamic military field of operations.

The major technical focus areas of the MEMS and Integrated Microsystems programs contained in this project are: 1) inertial measurement; 2) fluid sensing and control; 3) electromagnetic and optical beam steering; 4) chemical reactions on chip; 5) electromechanical signal processing; 6) analytical instruments; 7) thermal management; and 8) navigation and positioning technologies.

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2011 | FY 2012 | FY 2013 |
|---|---|---|---|
| ***Title:*** Thermal Management Technologies (TMT) | 27.797 | 19.936 | - |
| ***Description:*** The goal of the Thermal Management Technologies (TMT) program is to explore and optimize new nanostructured materials and other recent advances for use in thermal management systems. The overall goal of the program is to insert breakthrough materials and structures at all layers of DoD systems, and enable higher power densities, increased performance, and improved efficiency. Innovative research is underway to go beyond evolutionary thermal management systems. Modern, high-performance heat spreaders, which use two-phase cooling, are being developed to replace the copper alloy spreaders in conventional systems. Enhancing air-cooled exchangers by reducing the thermal resistance through the heat sink to the ambient, increasing convection through the system, improving heat sink fin thermal conductivity, optimizing and/or redesigning the complimentary heat sink blower, and increasing the overall system (heat sink and blower) coefficient of performance is another thrust of this program. Another element of this effort is focused on novel materials and structures that can provide significant reductions in the thermal resistance of the thermal interface layer between the backside of an electronic device and the next layer of the package, which might be a spreader or a heat sink. The TMT program is an aggregation of: Thermal Ground Plane | | | |

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| B. Accomplishments/Planned Programs ($ in Millions) | FY 2011 | FY 2012 | FY 2013 |
|---|---|---|---|
| (TGP), Microtechnologies for Air-Cooled Exchangers (MACE), Nano Thermal Interfaces (NTI) and Active Cooling Modules (ACM) technology research. Technology will be inserted through DoD industrial firms into future DoD systems.<br><br>***FY 2011 Accomplishments:***<br>- Delivered sample high thermal conductivity substrates to DoD labs (Army Research Laboratory, Naval Surface Warfare Center and the Air Force Research Laboratory) for testing against DoD application needs.<br>- Designed customized substrates for customer-selected insertion opportunities.<br>- Designed and built prototype active cooling module elements that demonstrate active cooler benefits.<br>- Delivered enhanced heat exchangers for insertion demonstrations on mobile platforms.<br>- Demonstrated reliable, reworkable nanostructured thermal interface materials based on nanotubes, nanoplates and nanosprings with reduced thermal resistance.<br><br>***FY 2012 Plans:***<br>- Insert TGP substrates to demonstrate improvements in Gallium Nitride Power amplifiers, High-Power transmit/receive modules, high-density electronic systems, avionics modules, and other opportunities enabled by lightweight, flexible, highly-conductive heat spreaders.<br>- Complete insertion demonstrations for enhanced heat exchangers, and initiate transitions to platforms.<br>- Demonstrate 10x improvements over state of the art for reworkable thermal interface materials.<br>- Demonstrate high active cooling modules for efficient operation of cooled electronic devices. | | | |
| ***Title:*** Micro-Technology for Positioning, Navigation, and Timing (Micro PN&T) | 33.698 | 42.117 | 36.466 |
| ***Description:*** The Micro-Technology for Positioning, Navigation, and Timing (Micro PN&T) program is developing technology for self-contained chip-scale inertial navigation and precision guidance. This technology promises to effectively mitigate dependence on Global Positioning System (GPS) or any other external signals, and enable uncompromised navigation and guidance capabilities. The program will enable positioning, navigation and timing functions without the need for external information updates by employing on-chip calibration, thereby overcoming vulnerabilities which arise in environments where external updates are not available such as caves, tunnels, or dense urban locations. The technologies developed will enable small, low-power, micro-gyroscopes capable of operating in both moderate and challenging dynamic environments; chip-scale primary atomic clock standards; and on-chip calibration systems for error correction. Advanced micro-fabrication techniques allow a single package containing all the necessary devices (clocks, accelerometers, gyroscopes, and calibration mechanisms) to be incorporated into a volume the size of a sugar cube. The small size, weight and power (SWaP) of these technologies and their integration into a single package responds to the needs of guided munitions, unmanned aerial vehicles (UAVs) and individual soldiers. The Micro PN&T program is an aggregation of Integrated Primary Atomic Clock, Navigate Grade Integrated Micromachined Gyroscopes, Micro Inertial Navigation Technology, Information Tethered Microscale Autonomous Rotary Stages, Micromachined Rate Integrating Gyroscopes, Single-Chip Timing and Inertial Measurement Unit, Primary and Secondary Calibration on Active | | | |

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| B. Accomplishments/Planned Programs ($ in Millions) | FY 2011 | FY 2012 | FY 2013 |
|---|---|---|---|

Layer, and Chip-Scale Combinatorial Atomic Navigator. The technology is expected to transition through industry and existing DoD transition partnerships with the Services.

To achieve the low SWaP necessary for guided munitions, UAVs, and personal navigation applications, the technologies in the MicroPN&T program will have to push the limitations of integration and performance in current MicroElectroMechanical systems (MEMS) technologies. Unprecedented levels of precision will be required to meet the stringent demands of the military environment. New architectures for devices will be developed that will leverage advances in fabrication techniques in order to increase stability and performance of a MEMS structure. Applied research for this program is funded within PE 0602716E, Project ELT-01.

***FY 2011 Accomplishments:***

- Transitioned chip-scale atomic clock effort to the Army's ManTech program.
- Demonstrated a 25cc cold atom micro-primary standard package that consumes only 150 Megawatts and has a time loss of 157 nanoseconds after one day.
- Demonstrated 4m @ 4hrs navigation accuracy during walking along a closed perimeter.
- Demonstrated 5cc nuclear magnetic resonance gyroscope that consumes 20mW of power and has a Angle Random Walk of 0.01 degrees per square root of hour and bias drift of 0.05 degrees per hour.
- Demonstrated 0.2 cc micro-stage rotating at 10 deg/sec and has a run time of 100 hrs.
- Demonstrated trapping 10^5 to 10^6 ions in the miniature ion trap 25 cc in volume consuming 150mW.
- Conducted independent government testing of chip-scale atomic clocks and micro-gyroscopes on a P-3 Orion and T-6B aircraft.

***FY 2012 Plans:***

- Develop design architecture for low-cost, small size rate integrating gyroscopes to provide direct measurement of orientation and angular velocity.
- Identify fabrication method to co-fabricate clocks and inertial sensors into a single low power package for navigation microsystems either monolithically or with disparate materials.
- Demonstrate three-dimensional microfabrication techniques for rate integrating gyroscopes that are compatible with large scale manufacturing.
- Model internal and external sources of error for inertial devices.
- Identify self-calibration techniques to compensate for long-term drift.

***FY 2013 Plans:***

- Demonstrate a microsystem rate integrating gyroscope to provide directly measured orientation angle and angular velocity.
- Demonstrate a microsystem that combines a functional timing and inertial measurement unit.

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| B. Accomplishments/Planned Programs ($ in Millions) | FY 2011 | FY 2012 | FY 2013 |
|---|---|---|---|
| - Demonstrate the co-fabrication of an inertial sensor and a calibration stage to enable integration of error correction technologies on the same stage.<br>- Demonstrate a fabrication technique that allows for the integration of timing and inertial measurement unit into a small package.<br>- Use models for internal and external sources of error to develop on-chip calibration algorithms.<br>- Develop an architecture for chip-scale combinatorial atomic navigator.<br>- Demonstrate combinatorial physics for fast startup time, high accuracy inertial devices. | | | |
| ***Title:*** MEMS Exchange<br><br>***Description:*** The MEMS Exchange program provided MEMS fabrication technology services to a broad user base, including all levels of industry and academia in support of Army, Navy, Air Force, and other DoD requirements. A major goal of the effort was to ensure self-sustained operation of the MEMS Exchange without further DARPA sponsorship. This program aided in the establishment of an accessible infrastructure for low or medium volume production of MEMS-enabled products for DoD applications.<br><br>***FY 2011 Accomplishments:***<br>- Implemented quality control efforts to achieve higher reliability in manufacturing.<br>- Optimized process cost efficiencies by increased marketing of MEMS Exchange capability.<br>- Improved self-sufficiency by providing a higher value to program users by improved yield and lower manufacturing costs. | 1.100 | - | - |
| ***Title:*** Chip-Scale Technology<br><br>***Description:*** The goal of the Chip-Scale Technology effort was to enhance microsystems performance by developing efficient on-chip vacuum pumps that meet application requirements for chip-scale micro-gas analyzers. Chip-Scale Technologies have the potential to improve the critical performance of microsystems such as micro mass spectrometers, nanoscale detectors, RF resonators, and vacuum microelectronic components. This program developed a high-performance integrated low-power (< 2 W) microscale (< 15 cm3) pumping (< 10-6 Torr) capability, and is transitioning via industrial performers.<br><br>***FY 2011 Accomplishments:***<br>- Demonstrated a microfabricated mid-vacuum turbomolecular pump with a 10^5 compression ratio, exceeding 10^-5 Torr while consuming < 1 W.<br>- Demonstrated Knudsen pump, requiring only 0.4 Watts to evacuate from 760 Torr to 7 Torr.<br>- Demonstrated Micro-scale sputter-ion pump evacuating down to 10^-2 Torr while consuming no more than 0.4 Watts.<br>- Demonstrated single-stage microfabricated rough pump with a compression ratio of 4.6 - this is the highest recorded value for a MEMS pump. | 7.414 | - | - |

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| B. Accomplishments/Planned Programs ($ in Millions) | FY 2011 | FY 2012 | FY 2013 |
|---|---|---|---|
| - Demonstrated meso-scale rough pump (23 cm^3) capable of sustaining mass-flow of 11 standard cubic centimeters per minute with 3.1 Watts of power. | | | |
| ***Title:*** Nano-Electro-Mechanical Computers (NEMS)<br><br>***Description:*** The goal of the Nano-Electro-Mechanical Computers (NEMS) program was to develop nanoscale mechanical switches and gain elements integrated intimately with complementary metal-oxide semiconductor switches. The program also developed mechanical gain elements to enable very low-noise, high-frequency amplifiers for low-power, low-noise analog signal processing. This technology will facilitate production of electronics that are less susceptible to electromagnetic pulse attacks and is transitioning into DoD systems via industrial program performers.<br><br>***FY 2011 Accomplishments:***<br>- Demonstrated digital building blocks for 4-bit and 8-bit mechanical microcontroller - finite state machines, counters, latches, registers, memory arrays, clocks, adders, and multipliers.<br>- Demonstrated automated design flow, logic synthesis, design rule checking and formal verification of complex relay-based very large scale integration circuits. Microcontroller design with 12,000 relays required only 5% hand-tuned custom logic design to minimize impact of mechanical delays.<br>- Demonstrated 10^7 cycles to failure when operating under realistic conditions.<br>- Demonstrated mixed-signal mechanical components - analog to digital converters, digital to analog converters, compressors, ring oscillators, real-time clock, and class E power amplifiers.<br>- Demonstrated reduced power consumption (3x) and footprint (2x) of Field Programmable Gate Array/mechanical switch hybrid technology without loss of speed - designed and fabricated in collaboration with a major FPGA manufacturer. | 7.170 | - | - |
| **Accomplishments/Planned Programs Subtotals** | 77.179 | 62.053 | 36.466 |

**C. Other Program Funding Summary ($ in Millions)**

N/A

**D. Acquisition Strategy**

N/A

**E. Performance Metrics**

Specific programmatic performance metrics are listed above in the program accomplishments and plans section.

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| COST ($ in Millions) | FY 2011 | FY 2012 | FY 2013 Base | FY 2013 OCO | FY 2013 Total | FY 2014 | FY 2015 | FY 2016 | FY 2017 | Cost To Complete | Total Cost |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MT-15: *MIXED TECHNOLOGY INTEGRATION* | 103.939 | 88.233 | 74.542 | - | 74.542 | 61.477 | 71.770 | 57.770 | 56.748 | Continuing | Continuing |

**A. Mission Description and Budget Item Justification**

The goal of the Mixed Technology Integration project is to leverage advanced microelectronics manufacturing infrastructure and DARPA component technologies developed in other projects to produce mixed-technology microsystems. These 'wristwatch size', low-cost, lightweight and low power microsystems will improve the battlefield awareness, security of the warfighter and the operational performance of military platforms. At the present time, systems are fabricated by assembling a number of mixed-technology components: microelectromechanical systems (MEMS), microphotonics, microfluidics and millimeterwave/microwave. Each technology usually requires a different level of integration, occupies a separate silicon chip and requires off-chip wiring, and requires fastening and packaging to form a module. The chip assembly and packaging processes produce a high cost, high power, large volume and lower performance system. This program is focused on the monolithic integration of mixed technologies to form batch-fabricated, mixed technology microsystems 'on-a-single-chip' or an integrated and interconnected 'stack-of-chips'.

The field of microelectronics incorporates micrometer/nanometer scale integration and is the most highly integrated, low-cost and high-impact technology to date. Microelectronics technology has produced the microcomputer-chip that enabled or supported the revolutions in computers, networking and communication. This program extends the microelectronics paradigm to include the integration of heterogeneous or mixed technologies. This new paradigm will create a new class of 'matchbook-size', highly integrated device and microsystem architectures. Examples of component-microsystems include low-power, small-volume, lightweight, microsensors, microrobots and microcommunication systems that will improve and expand the performance of the warfighter, military platforms, munitions and Unmanned Air Vehicles (UAVs).

The program includes the integration of mixed materials on generic substrates including glass, polymers and silicon. The program is design and process intensive, using 'standard' processes and developing new semiconductor-like processes and technologies that support the integration of mixed-technologies at the micrometer/ nanometer scale. The program includes the development of micrometer/nanometer scale isolation, contacts, interconnects and 'multiple-chip-scale' packaging for electronic, mechanical, fluidic, photonic and rf/mmwave/microwave technologies. For example, a mixed-technology microsystem using integrated microfluidics, MEMS, microphotonics, microelectronics and microwave components could provide a highly integrated, portable analytical instrument to monitor the battlefield environment, the physical condition of a warfighter, the identity of warfighters (friend or foe) or the combat readiness of equipment. The ability to integrate mixed technologies onto a single substrate will drive down the size, weight, volume, and cost of weapon systems while increasing their performance and reliability.

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2011 | FY 2012 | FY 2013 |
|---|---|---|---|
| ***Title:*** COmpact Ultra-stable Gyro for Absolute Reference (COUGAR) | 10.501 | 10.087 | - |
| ***Description:*** The COmpact Ultra-stable Gyro for Absolute Reference (COUGAR) program goal is to realize the fundamental performance potential of the resonant fiber optic gyro in combination with bandgap optical fiber (BGOF), ultra-stable compact lasers, phase conjugate elements, and silicon optical benches: a compact ultra-stable gyro for absolute reference applications. | | | |

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| B. Accomplishments/Planned Programs ($ in Millions) | FY 2011 | FY 2012 | FY 2013 |
|---|---|---|---|
| The COUGAR gyro will have a practical and typical size (~ 4 inch diameter) featuring bias stability and sensitivity (or angle random walk), which is more than 100 times better than state-of-the-art gyroscopes. This program will transition via industry.<br><br>***FY 2011 Accomplishments:***<br>- Reduced loss in BGOF to 0.6 decibels per kilometer (dB/km).<br>- Demonstrated laser with laser noise suppression electronics on lab bench.<br>- Developed initial Silicon optical bench interface for gyro based band gap optical fiber.<br>***FY 2012 Plans:***<br>- Develop bandgap optical fiber process to realize 500m lengths of polarizing bandgap fiber with less than 0.5 dB/m loss and off axis polarization suppression.<br>- Demonstrate low noise laser in package suitable for integration with final 4 in diameter gyro.<br>- Demonstrate bandgap optical fiber gyro in the laboratory using a 6 in coil with path to 4 in coil. | | | |
| ***Title:*** Gratings of Regular Arrays and Trim Exposures (GRATE)<br><br>***Description:*** The Gratings of Regular Arrays and Trim Exposures (GRATE) program will develop revolutionary circuit design methodologies combined with hybrid lithography tools to enable cost-effective low volume nanofabrication for DoD applications. Moore's law has driven the silicon industry for several decades with the minimum feature size on an integrated circuit (IC) reduced to 22 nm for today's commercial products. Due to challenging patterning requirements and complex circuitry, the costs of circuit design and verification, lithography tools and masks, and testing costs have increased exponentially and are unaffordable for low-volume manufacture of application specific integrated circuits (ASICs) for military electronics. Consequently, military electronics capabilities are currently limited by the high cost of nanofabrication. To solve this important problem, DARPA has invested in a variety of maskless patterning technologies including parallel e-beam arrays, parallel scanning probe arrays, and an innovative e-beam lithography tool. This program will develop revolutionary circuit design methodologies coupled with innovative fabrication techniques and hybrid maskless patterning tools to realize cost-effective nanofabrication for low-volume defense or commercial ASICs. Such an approach can also address the nanofabrication requirements of other low-volume DoD technologies such as photonics and micro-electro-mechanical systems. This program will transition via industry.<br><br>***FY 2011 Accomplishments:***<br>- Designed a set of logic and memory cells optimally suited to 1-D patterning at the 32 nanometers technology node using silicon test data directly from the fab.<br>- Demonstrated photolithography techniques for line widths < 32 nm by triple patterning and ~12.5 nm by using directed self-assembly (DSA) techniques.<br>- Completed initial exploration and evaluation studies of 1-D computer aided design tool development for extension to the 14 nm technology node. | 7.425 | 9.000 | 6.415 |

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| B. Accomplishments/Planned Programs ($ in Millions) | FY 2011 | FY 2012 | FY 2013 |
|---|---|---|---|
| - Completed preliminary 1-D fabrication demos including various circuit elements making use of 1-D specific process extensions.<br>- Demonstrated linewidths < 90 nm for analog devices using existing lithography tools and matched speed performance of state-of-the-art devices.<br>***FY 2012 Plans:***<br>- Demonstrate grating-based design and fabrication, including experimental verification of desired patterns. The demonstration vehicles will be logic/memory "standard cells" and high speed RF devices in state-of-the-art Complimentary Metal-Oxide Semiconductor (CMOS) technologies.<br>- Develop the "trim/stitch" processes for digital designs at 32 nm.<br>- Fabricate analog devices with > 350 GHz performance.<br>- Create a design targeted at 14nm technology for CMOS using basic library tools from phase 1.<br>***FY 2013 Plans:***<br>- Fabricate 1-D digital design at the 22 nm node.<br>- Demonstrate > 300 GHz performance for 1-D Silicon Germanium transistor circuit.<br>- Transition and make the analog 1-D design and fabrication available to the DoD user community via a multi-project wafer run. | | | |
| ***Title:*** Maskless Direct-Write Nanolithography for Defense Applications | 17.609 | 15.000 | 15.000 |
| ***Description:*** The Maskless Direct-Write Nanolithography for Defense Applications program will develop a maskless, direct-write lithography tool that will address both the DoD's need for affordable, high performance, Integrated Circuits (ICs) in small lots and the commercial market's need for highly customized, application-specific ICs. In addition, this program will provide a cost effective manufacturing technology for low volume nanoelectromechanical systems (NEMS) and nanophotonics initiatives within the DoD. Transition will be achieved by maskless lithography tools, installed in the Trusted Foundry and in commercial foundries, which will enable affordable incorporation of state-of-the-art semiconductor devices in new military systems, and allow for the cost-effective upgrade of legacy military systems.<br>***FY 2011 Accomplishments:***<br>- Designed, built and tested Generation 2 Column. This column increases beam current and wafer throughput by 2X at reduced blur.<br>- Designed, built and tested a 10 m/s rotary stage to hold six 300 mm wafers.<br>- Integrated electron beam column and rotary stage demonstrator platform.<br>- Fabricated a Dynamic Pattern Generator (DPG) structure comprising more than 1 million electrostatic lenslets.<br>- Designed, built and tested wafer metrology system.<br>- Designed, built and tested DPG data preparation system and data path. | | | |

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| B. Accomplishments/Planned Programs ($ in Millions) | FY 2011 | FY 2012 | FY 2013 |
|---|---|---|---|
| - Designed, built and tested Generation 3 Column. This column iteration further increases beam current and reduces blur.<br>***FY 2012 Plans:***<br>- Demonstrate system-level lithography achieving a resolution of <100 nanometers (nm) and a throughput of one 300mm-wafer-level-per-hour.<br>- Develop and demonstrate a sensitive photoresist with acceptable performance for the 32 nm node.<br>- Design and fabricate a second generation DPG alleviating processing challenges.<br>- Demonstrate and characterize layer-to-layer alignment and swath-to-swath stitching.<br>- Design and build final 100-150 kilo electron Volt e-beam column.<br>***FY 2013 Plans:***<br>- Design and build a high-throughput linear stage production platform.<br>- Demonstrate system-level lithography achieving a resolution of 45 nm and a throughput of 5-7 300mm-wafer-levels-per-hour.<br>- Make available Maskless Nanowriter lithography technology for incorporation into the DoD Trusted Foundry and other DoD foundries. | | | |
| ***Title:*** Advanced Wide FOV Architectures for Image Reconstruction & Exploitation (AWARE) | 33.217 | 15.946 | 12.198 |
| ***Description:*** The Advanced Wide FOV Architectures for Image Reconstruction & Exploitation (AWARE) program primarily addresses the passive imaging needs for multi-band, wide field of view (FOV) and high-resolution imaging for ground and near ground platforms. The AWARE program aims to solve the technological barriers that will enable wide FOV, high resolution and multi-band camera architectures by focusing on four major tasks: High space-bandwidth product (SBP) camera architecture; Small pitch pixel focal plane array architecture; Broadband focal plane array architecture; and Multi-band focal plane array architecture.<br><br>The AWARE program will advance integration of technologies that enable wide field of view and high resolution and multi-band cameras, including the technologies demonstrated in the related AWARE program in PE 0602716E, Project ELT-01. AWARE aggregates the following programs: Lambda Scale (formerly NIRD), Broadband (formerly PT-SQUAD), Multi-Band (formerly DUDE), and Wide Field of View (formerly MOSAIC). The integration of the technologies will demonstrate subsystems such as focal plane arrays (FPAs) and cameras.<br>***FY 2011 Accomplishments:***<br>- Demonstrated broadband detection from 0.5-5.0 micrometer (μm) with Noise Equivalent Temperature Difference (NETD) < 100 metre Kelvin (mK) at an operating temperature of 200 K using 30 μm photonic crystal array.<br>- Fabricated Long Wave Infrared (LWIR) 5μm detectors with performance and operability exceeding program goals.<br>- Demonstrated a 1280x720, 5 μm pixel Readout Integrated Circuit (ROIC) with a 75% warm probe yield. This will lead to low cost FPAs based on large number of die per wafer and excellent ROIC yield. | | | |

| Exhibit R-2A, RDT&E Project Justification: PB 2013 Defense Advanced Research Projects Agency | | DATE: February 2012 |
|---|---|---|
| APPROPRIATION/BUDGET ACTIVITY<br>0400: *Research, Development, Test & Evaluation, Defense-Wide*<br>BA 3: *Advanced Technology Development (ATD)* | R-1 ITEM NOMENCLATURE<br>PE 0603739E: *ADVANCED ELECTRONICS TECHNOLOGIES* | PROJECT<br>MT-15: *MIXED TECHNOLOGY INTEGRATION* |

| B. Accomplishments/Planned Programs ($ in Millions) | FY 2011 | FY 2012 | FY 2013 |
|---|---|---|---|
| - Established low temperature process for integrated dual band (LWIR and SWIR) IR detectors.<br>- Demonstrated independent functionality with integrated LWIR and SWIR detectors.<br>***FY 2012 Plans:***<br>- Develop and apply 10 µm pitch plated indium bump processes to electrically active ROIC wafers for hybridization to 512 x 512, 30µm photonic crystal pillar detector arrays.<br>- Develop photonic crystal FPA process scaling to 15µm pitch for 1.5K x 1k & 2k x 2k arrays.<br>- Start fabrication of 4:1 SWIR to LWIR device and demonstrate 4:1 architecture.<br>- Develop 720p 5 µm LWIR camera.<br>- Develop and fabricate 2k x 2k ROIC for LWIR camera to be assembled and demonstrated in 2013.<br>***FY 2013 Plans:***<br>- Fabricate 15µm pitch 1536x1024 FPA with Integrated Dewar Cooler Assembly (IDCA).<br>- Demonstrate integrated LWIR/SWIR camera (640x 512 for LWIR and 1024x1280 for SWIR).<br>- Demonstrate 2k x 2k, 5 µm LWIR pixel camera under brownout conditions. | | | |
| ***Title:*** Excalibur | 17.821 | 18.200 | 20.420 |
| ***Description:*** The Excalibur program will develop high-power electronically-steerable optical arrays, with each array element powered by a fiber laser amplifier. These fiber-laser arrays will be sufficiently lightweight, compact, and electrically efficient to be fielded on a variety of platforms with minimal impact to the platform's original mission capabilities. Each array element will possess an adaptive-optic capability to minimize beam divergence in the presence of atmospheric turbulence, together with wide-field-of-view beam steering for target tracking. With each Excalibur array element powered by high power fiber laser amplifiers (at up to 3 kilowatts per amplifier), high power air-to-air and air-to-ground engagements will be enabled that were previously infeasible because of laser system size and weight. In addition, this program will also develop kilowatt-class arrays of diode lasers which will provide an alternate route to efficiently reaching mission-relevant power levels, and they will test the ultimate scalability of the optical phased array architecture. Excalibur arrays will be conformal to aircraft surfaces and scalable in size and power by adding elements to the array. By defending airborne platforms such as unmanned aerial vehicles against proliferated, deployed, and next-generation man-portable air-defense systems (MANPADS), Excalibur will enable these reconnaissance platforms to fly at lower altitude and obtain truly persistent, all-weather ground reconnaissance despite low-lying cloud cover. Proliferated and emerging threats will be evaluated for the potential of developing a near-term capability utilizing a single high-power fiber laser amplifier. Further capabilities include multichannel laser communications, target identification, tracking, designation, precision defeat with minimal collateral effects as well as other applications.<br><br>The Excalibur program will also develop efficient high-power laser amplifier arrays based on coherent or spectral beam-combining. The potential of these arrays to scale to tactical power levels (100 kilowatt class) will be investigated. These laser | | | |

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| B. Accomplishments/Planned Programs ($ in Millions) | FY 2011 | FY 2012 | FY 2013 |
|---|---|---|---|
| amplifier arrays will be designed to work in tandem with the core laser components developed under the Excalibur program in PE 0602702E, Project TT-06. In addition prototype High Energy Laser Counter Measure (HELCM) systems will be developed to enable a near-term capability for low-altitude self-defense against MANPADS. This technology will transition via industry.<br><br>***FY 2011 Accomplishments:***<br>- Demonstrated phase locking and atmospheric compensation of turbulence on a 7-kilometer range using a 7-element optical phased array.<br>- Performed functional-defeat testing of representative proliferated and deployed MANPADS threats.<br>- Demonstrated a phased array of eight 500-W fiber laser amplifiers.<br>- Developed conceptual designs for complete high-energy laser countermeasure (HELCM) systems for both functional and structural kill that are compact and light enough to be deployed on Reaper-class UAVs.<br><br>***FY 2012 Plans:***<br>- Complete the design, fabricate and procure the components for a coherently or spectrally combinable array of 21 array elements, each fed by a compact 1-kW fiber laser amplifier.<br>- Demonstrate a 7-kW 7-element fiber-amplifier laser array using coherent-combining with a diffractive optical element, spectral-combining with a dispersive grating, and coherent-combining using a 2-D array with adaptive optics for tip/tilt correction.<br>- Initiate development of ancillary HELCM open architecture subsystems (command, threat warning/ laser-quality declaration, lightweight pod).<br><br>***FY 2013 Plans:***<br>- Demonstrate beam combining (coherent or spectral) of twenty-one 1-kW fiber laser amplifiers.<br>- Demonstrate coherent combining of a 19-element 2-D optical phased array with a combined power of 21 kW and tip/tilt adaptive optics.<br>- Develop and demonstrate prototype HELCM open-architecture subsystems in a laboratory environment.<br>- Initiate the development of a proactive search capability for HELCM systems. | | | |
| ***Title:*** Low Cost Thermal Imager - Manufacturing (LCTI-M) | 5.357 | 20.000 | 20.509 |
| ***Description:*** The Low Cost Thermal Imager - Manufacturing (LCTI-M) effort builds upon previous manufacturing and imaging work and will develop a pocket-sized, manufacturable, and practical thermal imager at a price point that allows them to be provided to large numbers of warfighters. Availability of very low cost and small form-factor infrared (IR) cameras will facilitate new techniques and applications that could provide the decisive edge needed in modern battlefields. These cameras will allow a soldier to have practical thermal imaging capability for locating warm objects (e.g., enemy combatants) in darkness. The small size, weight and power (SWaP) thermal camera will be integrated with a handheld device such as a cell phone with network capability for tactical intelligence, surveillance and reconnaissance. In order to achieve this goal, breakthroughs will be required | | | |

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| B. Accomplishments/Planned Programs ($ in Millions) | FY 2011 | FY 2012 | FY 2013 |
|---|---|---|---|
| in low-cost thermal imagers manufactured using wafer scale integration, vacuum packaging, low cost optics and low-power signal processing. By the end of the program, the imager chips will be fully integrated with a low-cost processor and optics. The camera will have wireless connectivity to integrate video display with cell phones or PDAs. U.S. Army PEO Soldier Sensors and Lasers (SSL), PM Optics USMC and industry will be the transition partners.<br><br>***FY 2011 Accomplishments:***<br>- Preliminary requirement analysis for the camera architecture completed.<br>- Phase I efforts by industry performers initiated to develop and fabricate components required for the low cost ($500) thermal imager.<br>- Developed a mini portable thermal camera as the initial benchmark and demonstration for size, weight and power.<br>- Handheld cellular phone platform selected as the portable display and computing engine.<br><br>***FY 2012 Plans:***<br>- Develop and review camera design and overall architecture compatible with cell phone platform.<br>- Develop and evaluate wafer-scale vacuum packaging of 17-micron bolometers with infrared-transparent windows.<br>- Develop low cost infrared optics and wafer scale camera electronics.<br><br>***FY 2013 Plans:***<br>- Develop and evaluate wafer-scale vacuum packaging of 12-micron bolometers with infrared-transparent windows.<br>- Evaluate low cost infrared optics and wafer scale camera electronics.<br>- Demonstrate integrated bolometer-based thermal imager chips with integral packaging.<br>- Demonstrate connectivity and display on a handheld device (cell phone). | | | |
| ***Title:*** Hemispherical Array Detector for Imaging (HARDI) | 2.870 | - | - |
| ***Description:*** The Hemispherical Array Detector for Imaging (HARDI) program exploited the benefits of a hemispherical imaging surface. The key concept is that a detector array can be fabricated on a hemispherical substrate using materials such as organic/inorganic semiconductors and that this array can be combined with a single simple lens to produce a wide field of view, small form factor camera that operates over a wide spectral range (400 nm to 1900 nm). Organic materials have been shown to have good electronic and optoelectronic properties including light emission and detection. Furthermore, in-plane organic/inorganic transistors can be incorporated for pre-processing of images. Patterning of these materials on the hemispherical surface has been demonstrated by utilizing maskless laser lithography. This program will transition to DoD systems through a demonstration of an array prototype developed by industrial contractors.<br><br>***FY 2011 Accomplishments:***<br>- Demonstrated a prototype 1 megapixel, 1 cm radius hemispherical focal plane array for the spectral range of 400-1900 nm. | | | |

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| B. Accomplishments/Planned Programs ($ in Millions) | FY 2011 | FY 2012 | FY 2013 |
|---|---|---|---|
| - Developed a lens specifically designed for the hemispherical focal plane array.<br>- Demonstrated a prototype f/1.4 camera with a 120 degree field of view with high reliability. | | | |
| ***Title:*** Radio Frequency Photonic Technology (RPT)<br><br>***Description:*** The Radio Frequency Photonics Technology (RPT) program developed components and microsystems to revolutionize deployed signal intelligence (SIGINT) gathering capabilities. The radio frequency (RF) spectrum contains innumerable friendly and adversarial signals of interest including: voice and data communications, electronic signatures, and navigation information. Conventional electronic systems are challenged in detecting weak signals in the presence of strong ones (low-linearity) across a broad range of frequencies (narrow-band). The RPT program efficiently captured all RF signals of interest by developing broad-band (>10 gigahertz) high-linearity (>70 decibels dynamic-range) optical components and microsystems. RPT enabled linear broadband microsystems such as remote links, channelizers, and analog-to-digital converters (ADCs). The RPT program reduced susceptibility to electronic attack, increased the probability-of-intercepting (POI) adversaries on their first-pulse transmission, and increased information awareness 1000-fold. This technology will transition via industry.<br><br>***FY 2011 Accomplishments:***<br>- Developed photodiodes capable of 27.4 decibels per milliwatt RF power with a 15 GHz bandwidth.<br>- Demonstrated a photonic link with >120 dB/Hz2/3 SFDR from 9-17 GHz, a dynamic range 4 times better than a state-of-the-art electronics link. | 9.139 | - | - |
| **Accomplishments/Planned Programs Subtotals** | 103.939 | 88.233 | 74.542 |

**C. Other Program Funding Summary ($ in Millions)**

N/A

**D. Acquisition Strategy**

N/A

**E. Performance Metrics**

Specific programmatic performance metrics are listed above in the program accomplishments and plans section.