Exhibit R-2, RDT&E Budget Item Justification: PB 2012 Defense Advanced Research Projects Agency										DATE: February 2011	
APPROPRIATION/BUDGET ACTIVITY 0400: *Research, Development, Test & Evaluation, Defense-Wide* BA 2: *Applied Research*				R-1 ITEM NOMENCLATURE PE 0602716E: *ELECTRONICS TECHNOLOGY*							
COST ($ in Millions)	**FY 2010**	**FY 2011**	**FY 2012 Base**	**FY 2012 OCO**	**FY 2012 Total**	**FY 2013**	**FY 2014**	**FY 2015**	**FY 2016**	**Cost To Complete**	**Total Cost**
Total Program Element	184.188	286.936	215.178	-	215.178	204.416	194.518	197.900	212.900	Continuing	Continuing
ELT-01: *ELECTRONICS TECHNOLOGY*	184.188	286.936	215.178	-	215.178	204.416	194.518	197.900	212.900	Continuing	Continuing

A. Mission Description and Budget Item Justification

This program element is budgeted in the Applied Research budget activity because its objective is to develop electronics that make a wide range of military applications possible.

Advances in microelectronic device technologies, including digital, analog, photonic and MicroElectroMechanical Systems (MEMS) devices, continue to have significant impact in support of defense technologies for improved weapons effectiveness, improved intelligence capabilities and enhanced information superiority. The Electronics Technology program element supports the continued advancement of these technologies through the development of performance driven advanced capabilities, exceeding that available through commercial sources, in electronic, optoelectronic and MEMS devices, semiconductor device design and fabrication techniques, and new materials and material structures for device applications. A particular focus for this work is the exploitation of chip-scale heterogeneous integration technologies that permit the optimization of device and integrated module performance.

The phenomenal progress in current electronics and computer chips will face the fundamental limits of silicon technology in the early 21st century, a barrier that must be overcome in order for progress to continue. Another thrust of the program element will explore alternatives to silicon-based electronics in the areas of new electronic devices, new architectures to use them, new software to program the systems, and new methods to fabricate the chips. Approaches include nanotechnology, nanoelectronics, molecular electronics, spin-based electronics, quantum-computing, new circuit architectures optimizing these new devices, and new computer and electronic systems architectures. Projects will investigate the feasibility, design, and development of powerful information technology devices and systems using approaches for electronic device designs that extend beyond traditional Complementary Metal Oxide Semiconductor (CMOS) scaling, including non silicon-based materials technologies to achieve low cost, reliable, fast and secure computing, communication, and storage systems. This investigation is aimed at developing new capabilities from promising directions in the design of information processing components using both inorganic and organic substrates, designs of components and systems leveraging quantum effects and chaos, and innovative approaches to computing designs incorporating these components for such applications as low cost seamless pervasive computing, ultra-fast computing, and sensing and actuation devices.

This project has five major thrusts: Electronics, Photonics, MicroElectroMechanical Systems, Architectures, Algorithms, and other Electronic Technology research.

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B. Program Change Summary ($ in Millions)	FY 2010	FY 2011	FY 2012 Base	FY 2012 OCO	FY 2012 Total
Previous President's Budget	179.402	286.936	348.377	-	348.377
Current President's Budget	184.188	286.936	215.178	-	215.178
Total Adjustments	4.786	-	-133.199	-	-133.199
• Congressional General Reductions		-			
• Congressional Directed Reductions		-			
• Congressional Rescissions	-	-			
• Congressional Adds		-			
• Congressional Directed Transfers		-			
• Reprogrammings	9.545	-			
• SBIR/STTR Transfer	-4.759	-			
• TotalOtherAdjustments	-	-	-133.199	-	-133.199

Congressional Add Details ($ in Millions, and Includes General Reductions)	FY 2010	FY 2011
Project: ELT-01: *ELECTRONICS TECHNOLOGY*		
Congressional Add: *3-D Technology for Advanced Sensor Systems*	2.000	-
Congressional Add Subtotals for Project: ELT-01	2.000	-
Congressional Add Totals for all Projects	2.000	-

Change Summary Explanation

FY 2010: Increase reflects internal below threshold reprogramming offset by SBIR/STTR transfer.

FY 2012: Decrease reflects repricing of on-going electronics efforts following program aggregations and transition of energy-related electronics to the new tactical and strategic energy project (MBT-03) in PE 0602715E and Defense Efficiencies for contractor staff support.

C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
Title: Quantum Information Science (QIS)	3.416	10.641	4.700
Description: The Quantum Information Science (QIS) program will explore all facets of the research necessary to create new technologies based on quantum information science. Research in this area has the ultimate goal of demonstrating the potentially significant advantages of quantum mechanical effects in communication and computing. Expected applications include: new improved forms of highly secure communication; faster algorithms for optimization in logistics and wargaming; highly precise measurements of time and position on the earth and in space; and new image and signal processing methods for target tracking. Technical challenges include: loss of information due to quantum decoherence; limited communication distance due to signal			

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
attenuation; limited selection of algorithms and protocols; and larger numbers of bits. Error correction codes, fault tolerant schemes, and longer decoherence times will address the loss of information. Signal attenuation will be overcome by exploiting quantum repeaters. New algorithm techniques and complexity analysis will increase the selection of algorithms, as will a focus on signal processing. The QIS program is a broad-based effort that will continue to explore the fundamental open questions, the discovery of novel algorithms, and the theoretical and experimental limitations of quantum processing as well as the construction of efficient implementations. ***FY 2010 Accomplishments:*** - Measured single electron spin lifetime and demonstrated controlled gate operations in gated quantum dots (QD) in silicon (Si). - Conducted theoretical analysis of improvement in decoherence time resulting from dynamical decoupling schemes. - Explored novel materials, noise characteristics and decoherence mitigation strategies for superconducting qubits. ***FY 2011 Plans:*** - Measure single electron spin decoherence time in gated QD in Si. - Demonstrate entanglement swapping protocol in three QD quantum devices in Si. - Perform state tomography and dispersive readout for one and two superconducting qubits. - Fabricate high quality superconducting tunnel junctions through material improvement. ***FY 2012 Plans:*** - Demonstrate interconversion of quantum information from one type to another. - Demonstrate transport of quantum information over microscopic scales.			
Title: Terahertz Electronics ***Description:*** Terahertz Electronics will develop the critical semiconductor device and integration technologies necessary to realize compact, high-performance microelectronic devices and circuits that operate at center frequencies exceeding 1 Terahertz (THz). There are numerous benefits to operating in the THz regime and multiple new applications in imaging, radar, communications, and spectroscopy, all enabled by electronics that operate in the THz frequency regime. The Terahertz Electronics program is divided into two major technical activities: Terahertz Transistor Electronics that includes the development and demonstration of materials and processing technologies for transistors and integrated circuits for receivers and exciters that operate at THz frequencies; and Terahertz High Power Amplifier Modules that includes the development and demonstration of device and processing technologies for high power amplification of THz signals in compact modules. ***FY 2010 Accomplishments:*** - Developed devices and circuits for candidate applications with demonstration of operation at a frequency of at least 0.67 THz.	15.251	18.053	16.330

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
- Demonstrated 14dBm power amplification at 0.67 THz. ***FY 2011 Plans:*** - Achieve key device and integration technologies to realize compact, high performance electronic circuits operating beyond 0.85 THz. ***FY 2012 Plans:*** - Achieve key device and integration technologies to realize compact, high performance electronic circuits operating beyond 1.03 THz.			
Title: High Frequency Integrated Vacuum Electronic (HiFIVE) ***Description:*** The objective of the High Frequency Integrated Vacuum Electronic (HiFIVE) program is to develop and demonstrate new high-performance and low-cost technologies for implementing high-power millimeter-wave sources and components. This program is developing new semiconductor and micro-fabrication technologies to produce vacuum electronic high-power amplifiers for use in high-bandwidth, high-power transmitters. Innovations in design and fabrication are being pursued to enable precision etching, deposition, and pattern transfer techniques to produce resonant cavities, electrodes, and magnetics, and electron emitting cathodes for compact high-performance millimeter wave devices. These new technologies will eliminate the limitations associated with the conventional methods for assembly of high-power sources in this frequency range. ***FY 2010 Accomplishments:*** - Validated the design of a high-power amplifier through experiments and computational simulation. - Completed development of the high-performance cathode prototype and demonstrated its ability to operate without degradation for at least 1,000 hours. ***FY 2011 Plans:*** - Complete advanced cathode development activities. - Complete fabrication and initial testing of a high-power amplifier prototype device incorporating HiFIVE micro-fabrication technologies into a compact module form factor. - Initiate efforts to perform laboratory measurements of performance. ***FY 2012 Plans:*** - Demonstrate integrated and compact amplifier technology at G-band in a tube form factor. - Complete laboratory measurements of performance of miniaturized tube amplifier at 220GHz.	11.080	11.500	3.540
Title: Systems of Neuromorphic Adaptive Plastic Scalable Electronics (SyNAPSE)	17.025	27.608	31.000

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
Description: The vision of the Systems of Neuromorphic Adaptive Plastic Scalable Electronics (SyNAPSE) program is the development of biological-scale neuromorphic electronic systems for autonomous, unmanned, robotic systems where humans are currently the only viable option. The successful development of this technology will revolutionize warfare by providing intelligent terrestrial, underwater, and airborne systems that remove humans from dangerous environments and remove the limitations associated with today's remote-controlled robotic systems. Applications for neuromorphic electronics include not only robotic systems, but also natural human-machine interfaces and diverse sensory and information integration applications in the defense and civilian sectors. If successful, the program will also reinvigorate the maturing microelectronics industry by enabling a plethora of computer and consumer electronics applications. ***FY 2010 Accomplishments:*** - Developed a brain-inspired neuromorphic architectural design and specification capability. - Developed software tools to translate neuromorphic designs into electronic implementations using hybrid Complementary Metal-Oxide Semiconductor (CMOS) and high-density electronic synapse components. - Developed capability to simulate the performance of neuromorphic electronics systems using very large scale computation. - Developed virtual reality environments intended for training and evaluating electronic neuromorphic systems and their corresponding computer simulations. - Developed standard testing protocols for assessing the performance of large neuromorphic electronic systems. ***FY 2011 Plans:*** - Demonstrate all core microcircuit functions in hybrid CMOS electronic synapse hardware. - Demonstrate a dynamic neural system simulation of approximately one million neurons that shows plasticity, self-organization, and network stability in response to sensory stimulus and system level reinforcement. - Develop tools to design electronic neuromorphic systems of 100 billion neurons with mammalian connectivity. - Demonstrate virtual environments with a selectable range of complexity across the cognitive capabilities of small to medium sized mammals. - Specify a chip fabrication process supporting 1 million neurons per square centimeter and ten billion synapses per square centimeter. ***FY 2012 Plans:*** - Design and simulate in software a complete neural system of ~10 billion synapses and ~1 million neurons performing cognitive tasks in a virtual environment comparable to those routinely tested in mice. - Design and verify a hardware neural system of ~10 billion synapses and ~1 million neurons. - Demonstrate a chip fabrication process and development plan supporting ~10 billion synapses per square centimeter and ~1 million neurons per square centimeter.			

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
- Refine design tools and techniques by codifying design rules and component properties and matching them to fabrication and simulation capabilities. - Demonstrate a virtual environment supporting visual perception, decision and planning, and navigation environments fully integrated with software or hardware neural systems enabling the testing, training, and evaluation of these neural systems. - Expand the feature set of the virtual environment to include auditory perception and proprioception. - Introduce modalities of competition within the virtual environment to further tailor the evolution of the neural systems.			
Title: Short-range Wide-field-of-regard Extremely-agile Electronically-steered Photonic Emitter and Receiver (SWEEPER) ***Description:*** The objective of the Short-range Wide-field-of-regard Extremely-agile Electronically-steered Photonic Emitter and Receiver (SWEEPER) program is to develop chip-scale dense waveguide modular technology to achieve true embedded phase array control for beams equivalent to 10W average power, less than 0.1 degree instantaneous field of view (IFOV), greater than 45 degree total field of view (TFOV), and frame rates of greater than 100 Hertz (Hz) in packages that are "chip-scale." Such performance will represent a three order of magnitude increase in speed, while also achieving a greater than two orders of magnitude reduction in size. Additionally, the integrated phase control will provide the unprecedented ability to rapidly change the number of simultaneous beams, beam profile, and power-per-beam, thus opening a whole new direction in operational capability. Key technical challenges include the ability to achieve the needed facet density (facet pitch should be on the order of a wavelength or two), control the relative phase across all facets equivalent to 9-bits, and efficiently couple and distribute coherent light to facets from a master laser oscillator with an integrated waveguide structure. Related projects and studies have pointed to the significant system-level pay-offs of the new proposed technology. ***FY 2010 Accomplishments:*** - Evaluated transmit and receive photonic phased array technologies. ***FY 2011 Plans:*** - Demonstrate chip scale beam-forming capability in laboratory. - Demonstrate integrated photonic phased array transceiver concept. ***FY 2012 Plans:*** - Demonstrate 8x8 integrated photonic chip scale array beam forming with path towards 32x32 array. - Demonstrate 10°x10° beam steering with <20dB sidelobes.	2.800	8.800	6.000
Title: Electric Field Detector (E-FED) ***Description:*** The goal of the Electric Field Detector (E-FED) program is to develop a small room temperature electric field sensor/ sensor array based on new optical electric field sensor architectures. Electric fields are ubiquitous in the warfighter environment.	3.807	4.295	2.304

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
It is expected that these compact sensor arrays will be useful for the monitoring of brain activity and muscle action without the need to apply electrodes directly in or on the surface of the skin. The arrays would also be useful for the remote sensing of electronics, motors, and communications devices enabling the sensing of these devices at greater distances with a more unobtrusive and portable system. ***FY 2010 Accomplishments:*** - Designed and modeled miniature electric field sensors with high sensitivity to alternating electric fields. ***FY 2011 Plans:*** - Demonstrate sensors sensitive to an alternating electric field of 1 millivolt (mV)/meter root Hertz from 1-10,000 Hertz (Hz). - Develop techniques to increase the frequency range, dynamic range and sensitivity of the electric field sensors while reducing their size. - Explore manufacturing techniques in order to produce electric field sensor arrays with high reproducibility. ***FY 2012 Plans:*** - Demonstrate a sensor array with at least 25 elements with high sensitivity to an alternating electric field. - Demonstrate sensors sensitive to an alternating electric field of 1 microvolt (μV)/meter root Hertz from 0.5-1,000,000 Hertz (Hz).			
Title: Self-HEALing mixed-signal Integrated Circuits (HEALICs) ***Description:*** The goal of the Self-HEALing mixed-signal Integrated Circuits (HEALICs) program is to develop technologies to autonomously maximize the number of fully operational mixed-signal systems-on-a-chip (SoC) per wafer that meet all performance goals in the presence of extreme process technology variations, environmental conditions, and aging. Virtually all DoD systems employ mixed-signal circuits for functions such as communications, radar, navigation, sensing, high-speed image and video processing. A self-healing integrated circuit is defined as a design that is able to sense undesired circuit/system behaviors and correct them automatically. As semiconductor process technologies are being scaled to even smaller transistor dimensions, there is a dramatic increase in intra-wafer and inter-die process variations, which have a direct impact on realized circuit performance, as well as significantly increased sensitivity to temperature and ageing effects. The core goal of the HEALICs program is to regain this lost performance and stabilize operation over system lifetimes. Consequently, the long-term reliability of DoD electronic systems is expected to be significantly enhanced. ***FY 2010 Accomplishments:*** - Continued development of self-healing mixed-signal cores.	13.819	15.540	12.111

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
- Demonstrated increase in performance yield of mixed-signal cores to greater than seventy-five percent with minimal power and die area overhead. ***FY 2011 Plans:*** - Integrate previously demonstrated mixed-signal cores into a full microsystem/SoC. - Develop global self-healing control at the microsystem/SoC level. - Demonstrate simulated increase in performance yield of mixed-signal SoCs to greater than ninety-five percent with minimal power and die area overhead. - Continue development of self-healing IP core library for DoD user access. ***FY 2012 Plans:*** - Demonstrate increase in performance yield of fabricated mixed-signal SoCs to greater than ninety-five percent with minimal power and die area overhead. - Develop a full self-healing IP core library for DoD user access.			
Title: Efficient Linearized All-Silicon Transmitter ICs (ELASTx) ***Description:*** The goal of the Efficient Linearized All-Silicon Transmitter ICs (ELASTx) program is the development of revolutionary high-power/high-efficiency/high-linearity single-chip millimeter (mm)-wave transmitter integrated circuits (ICs) in leading edge silicon technologies. The high levels of integration possible in silicon technologies enable on-chip linearization, complex waveform synthesis, and digital calibration and correction. Military applications include ultra-miniaturized transceivers for satellite communications-on-the-move, collision avoidance radars for micro-/nano-air vehicles, and ultra-miniature seekers for small munitions. The technology developed under this program could also be leveraged to improve the performance of high-power amplifiers based-on other nonsilicon technologies through heterogeneous integration strategies. Significant technical obstacles to be overcome include the development of highly efficient circuits for increasing achievable output power of silicon devices (e.g., device stacking, power combining) at mm-waves; scaling high-efficiency amplifier classes to the mm-wave regime; integrated linearization architectures for complex modulated waveforms; and robust RF/mixed-signal isolation strategies. ***FY 2010 Accomplishments:*** - Initiated development of Watt-level, high power added efficiency (PAE) silicon-based power amplifier (PA) circuits at Q-band frequencies. - Initiated development of linearized transmitter circuits based on high PAE PAs at Q-band frequencies. - Initiated development of measurement techniques for mm-wave linearized transmitter circuits with complex modulated waveforms. ***FY 2011 Plans:***	7.436	9.491	6.306

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
- Demonstrate Watt-level, high PAE silicon-based PA circuits at Q-band frequencies. - Demonstrate linearized transmitter circuits based on high PAE PAs at Q-band frequencies with complex modulated waveforms. ***FY 2012 Plans:*** - Initiate development of Watt-level, high PAE silicon-based PA circuits at W-band frequencies. - Initiate development of linearized transmitter circuits based on high PAE PAs at W-band frequencies.			
Title: Compact Mid-Ultraviolet Technology ***Description:*** The goal of the Compact Mid-Ultraviolet Technology program is to develop compact high-brightness Middle Ultraviolet source and detector technologies based on wide band gap diode structures. This program will address a critical technology shortfall preventing mid-UV capability in portable chem-bio defense systems for aerosol detection (enhanced capability for small particulates), chem-bio identification (Raman scattering and spectroscopy), and chemical decontamination/water purification applications. The technologies will also address solar-blind detectors for missile plume identification. ***FY 2010 Accomplishments:*** - Initiated developments for large non-absorbing (UV transparent) low-defect-density substrate materials on which to grow devices. - Initiated high-quality, highly-strained epitaxy developments to confine carriers and provide the required energy band offsets. - Initiated highly efficient electric injection of carriers to improve quantum efficiency. - Initiated low-resistance non-absorbing contacts. ***FY 2011 Plans:*** - Demonstrate diode operation at proposed mid-UV wavelength. - Create high-quality aluminum nitride substrates and ternary templates to enable development of optimized devices. - Design and develop epitaxial structures for mid-UV light-emitting diode (LED) sources and detectors. ***FY 2012 Plans:*** - Demonstrate high wall plug efficiency, high brightness LED operating between 250-270nm. - Demonstrate 5mW semiconductor lasers operating below 250nm in wavelength.	7.798	15.400	15.000
Title: Adaptive Radio Frequency Technology (ART) ***Description:*** There is a critical ongoing military need for flexible, affordable, hand-held cognitive military communications systems. The Adaptive Radio Frequency Technology (ART) program will provide the warfighter with a new, fully adaptive radio platform capable of sensing the electromagnetic and waveform environment in which it operates, making decisions on how to best communicate in that environment, and rapidly adapting its hardware to meet ever-changing requirements, while simultaneously	6.763	17.619	16.918

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
significantly reducing the size, weight and power (SWAP) of such radio nodes. ART will also equip each warfighter, as well as small-scale unmanned platforms, with a compact and efficient signal identification capabilities for next-generation cognitive communications, sensing and electronic warfare applications. ART technology will also enable rapid radio platform deployment for new waveforms and changing operational requirements. ART aggregates the Feedback Linearized Microwave Amplifiers program, the Analog Spectral Processing program, and Chip Scale Spectrum Analyzers (CSSA) program, and initiates new thrusts in Cognitive Low-energy Signal Analysis and Sensing Integrated Circuits (CLASIC) and RF Field-Programmable Arrays (RF-FPGA). ***FY 2010 Accomplishments:*** - Demonstrated feedback-linearized InP HBT monolithic low-noise amplifiers with improved third-order-intercept point and noise figure. - Demonstrated feedback linearized InP HEMT monolithic low-noise amplifiers. - Demonstrated miniaturized, low-loss, tunable and reconfigurable RF and IF sensor filter banks. ***FY 2011 Plans:*** - Extend feedback linearized amplifier approaches to analog/RF applications such as active impedance matching of electrically small antennas, and initiate transition activities to signal intelligence and electronic warfare platforms. - Initiate development of novel signal recognition sensor integrated circuits that can achieve >400 times reduction in signal recognition energy as compared to state of the art sensor systems. - Initiate development of reconfigurable RF circuit (RF FPGA) technologies. ***FY 2012 Plans:*** - Continue development of novel signal recognition sensor integrated circuits. - Continue development of reconfigurable RF circuit (RF FPGA) technologies.			
Title: Nitride Electronic NeXt-Generation Technology (NEXT) ***Description:*** The objective of the Nitride Electronic NeXt-Generation Technology (NEXT) program is to develop a revolutionary nitride transistor technology that simultaneously provides extremely high-speed and high-voltage swing [Johnson Figure of Merit (JFoM) larger than 5 THz-V] in a process consistent with large scale integration in enhancement /depletion (E/D) mode logic circuits of 1000 or more transistors. In addition, this fabrication processes will be manufacturable, high-yield, high-uniformity, and highly reliable. The accomplishment of this goal will be validated through the demonstration of specific Program Process Control Monitor (PCM) Test Circuits such as 5, 51, and 501-stage of ring oscillators in each program phase. The NEXT program was previously included in the High Frequency Wide Band Gap Semiconductor program. ***FY 2010 Accomplishments:***	7.221	12.717	16.130

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
- Developed self-aligned structure with short gate length, novel barrier layers and reduced parasitics. - Demonstrated technologies to achieve circuits of significant complexity (1,000 transistor devices or more). - Developed transistor models. ***FY 2011 Plans:*** - Develop high-performance Gallium Nitride Field Effect Transistors (FETs). - Achieve yield to enable modest integration levels. - Demonstrate superior thermal management and packaging strategies. - Demonstrate self-aligned structure with short gate length, novel barrier layers and reduced parasitics. - Optimize transistor performance to include ultra-fast power switching capability. - Develop an optimized enhancement mode power switch process to complement high frequency FET process. - Design an integrated process for power switching and MMIC capability using advanced wide band gap devices. ***FY 2012 Plans:*** - Develop complex analog and digital monolithically integrated circuits based on next generation gallium nitride transistors and integration processes.			
Title: Non-Volatile Logic ***Description:*** The objective of the Non-Volatile Logic program is to develop the theory, design, and fabrication methodology, and demonstrate example circuits that utilize new computational state variables. The program will fabricate and demonstrate circuits that dissipate lower power, per logic operation, while having equal or better computational throughput as equivalent charge-based circuits. Non-Volatile Logic is an outgrowth of the Spin Torque Transfer Random Access Memory program. ***FY 2010 Accomplishments:*** - Initiated design and development of non-volatile logic gates and computational circuits to exploit new nano-magnet and electron spin state variables. - Demonstrated zero off-state power and reconfigurable majority logic gates with significantly reduced energy consumption relative to state-of-the-art Complementary Metal-Oxide Semiconductor (CMOS) logic gates. ***FY 2011 Plans:*** - Develop circuits capable of performing logic functions based on the nano-magnetic re-orientation information and not on the movement of electrical charge. - Develop fabrication techniques to make nano-magnetic based logic devices. ***FY 2012 Plans:***	4.750	7.911	5.839

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
- Demonstrate a simple computational circuit based on magnetic orientation information that can switch in 10 nanoseconds and that utilizes less than 100 attojoules per switch. - Demonstrate the non-volatility of information in the fabricated circuit.			
Title: Photonically Optimized Embedded Microprocessor (POEM) ***Description:*** Current trends in scaling microprocessor performance are projected to saturate and fall far short of future military needs. Microprocessor performance is saturating and leading to reduced computational efficiency because of the limitations of electrical communications. The Photonically Optimized Embedded Microprocessor (POEM) program will demonstrate chip-scale, silicon-photonic technologies that can be integrated within embedded microprocessors for seamless, energy-efficient, high-capacity communications within and between the microprocessor and Dynamic random access memory (DRAM). This technology will propel microprocessors onto a higher performance trajectory by overcoming the "memory wall", and thus satisfy projected microprocessor performance needs for memory intensive applications. This program aggregated Advanced CAD, Non-Silicon Electronics and Terahertz Photonics plus Advanced Photonic Switch (APS), Photonic Integrated Circuits on Silicon (EPIC), Ultradense Nanophotonic Intra chip Communications (UNIC) previously reported in PE 0603739E, Project MT-15. ***FY 2010 Accomplishments:*** - Demonstrated the world's lowest power photonic transmitter, comprised of Complementary Metal-Oxide semiconductor (CMOS)-compatible Si photonic devices and electronic drivers, and operating at 5 gigabits/second (Gb/s), with an efficiency of 400 fJ/bit (energy scatter) (unit time). - Demonstrated the world's lowest power digital, optical receiver, comprised of a CMOS-compatible, Ge-on-Si-based photodetector with associated circuitry, and operating at 5 Gb/s, with an efficiency of 690 fJ/bit. - Demonstrated a low power, thermally tolerant, 2x2 port, switch device with 110 nano meter (nm) switching bandwidth and 160 Gb/s throughput. ***FY 2011 Plans:*** - Develop CMOS-compatible modulator, multiplexor, coupler, and photodetector devices for low-power, high capacity photonic links. - Develop DRAM-compatible modulator, multiplexor, coupler, and photodetector devices for low-power, high capacity photonic links. - Develop CMOS-compatible, waveguide coupled, high-gain-bandwidth avalanche photodiodes for high speed operation. - Develop low power, thermally tolerant, switch devices with >30 nm switching bandwidth. ***FY 2012 Plans:*** - Demonstrate a CMOS-compatible 300 fJ/bit photonic link with 120 Gb/s capacity.	13.333	21.965	28.000

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
- Demonstrate a DRAM-compatible 1500 fJ/bit photonic link with 80 Gb/s capacity. - Demonstrate CMOS-compatible, waveguide coupled, high-gain-bandwidth avalanche photodiodes which operate at 40 Gb/s. - Demonstrate a low power, thermally tolerant, 8x8 port, switch device with >30 nm switching bandwidth and 800 Gb/s throughput.			
Title: Compound Semiconductor Materials On Silicon (COSMOS)	6.700	15.900	8.000
Description: Conventional integrated circuit processing is limited to one type of semiconductor material but many DoD systems have circuits based on multiple types of semiconductor devices. Consequently, these diverse devices and circuits are assembled together on printed circuit boards or in multi-chip modules. This conventional approach suffers from degraded performance at high-speed/RF frequencies due to parasitic and signal path delays, and increased costs due to packaging and module assembly steps. The objective of the Compound Semiconductor Materials On Silicon (COSMOS) program is to develop robust, high-yield semiconductor fabrication technologies and manufacturing processes for the intimate heterogeneous integration of multiple types of devices and semiconductor materials, specifically III-V compound semiconductor (CS) devices into high-density silicon Complementary Metal-Oxide Semiconductor (CMOS) platforms. This capability enables designers to leverage the high-speed and high-breakdown voltage of CS devices where most appropriate, while exploiting the complexity of advanced silicon CMOS for in situ calibration, linearization and signal processing - i.e. the principle of "best junction for the function". Based on this approach, the COSMOS program is specifically developing high-speed, high-linearity mixed-signal designs such as digital-to-analog converters and analog-to-digital converters with revolutionary performance for future military communications, sensing and electronic warfare systems. ***FY 2010 Accomplishments:*** - Increased the density of heterogeneous interconnections between compound semiconductor and silicon devices. - Implemented process enhancements to improve the yield of the heterogeneous integration process. - Initiated design and fabrication of an advanced mixed-signal circuit demonstrator, a heterogeneously-integrated wideband, ultra-high-linearity digital-to-analog converter with in situ silicon enabled calibration and linearization. ***FY 2011 Plans:*** - Complete and test an advanced mixed-signal circuit demonstrator, a heterogeneously-integrated wideband, ultra-high-linearity digital-to-analog converter with in situ silicon enabled calibration and linearization. - Initiate design of a higher complexity mixed signal circuit demonstrator, a heterogeneously-integrated wideband, ultra-high-linearity analog-to-digital converter with in situ silicon enabled calibration and linearization.			

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
- Optimize the COSMOS process to demonstrate that fine-scale heterogeneous integration can be realized on a large-scale circuit with high manufacturing and performance yield. ***FY 2012 Plans:*** - Continue design, fabrication and test of a higher complexity mixed signal circuit demonstrator, a heterogeneously-integrated wideband, ultra-high-linearity analog-to-digital converter with in situ silicon enabled calibration and linearization. - Continue COSMOS process yield and robustness enhancement.			
Title: Analog-to-Information (A-to-I) Receiver Development ***Description:*** The Analog-to-Information (A-to-I) Receiver Development program will fundamentally improve the operational bandwidth, linearity, and efficiency of electronic systems where the objective is to receive and transmit information using electromagnetic (radio) waves under extreme size/weight/power and environmental conditions required for DoD applications. The A-to-I Look-Through program will develop ultra-wideband digital radio frequency (RF) receivers based on Analog-to-Information Converter (AIC) technology. Compared to conventional RF receivers, AIC-based designs will increase receiver dynamic range and frequency band of regard while reducing data glut, power consumption and size. Likewise, limitations of current art power amplifier technology in simultaneously achieving high operational bandwidth, linearity, efficiency and power has resulted in well documented instances of electronic fratricide. This program will overcome these limitations by converting digital signals directly to high power RF analog signals, thus eliminating the traditional high power amplifiers that are limited by the above-mentioned tradeoffs. Transition is anticipated into airborne SIGINT and electronic warfare systems, as well as ground-based special operations forces systems. ***FY 2010 Accomplishments:*** - Demonstrated effectiveness of 2x to 20x Nyquist sub-sampling and addressed critical issues regarding noise. - Developed and demonstrated novel mathematical algorithms to rapidly process sub-Nyquist data, improving execution time for signal detection, identification, and reconstruction. - Completed prototypes of critical receiver hardware components for A-to-I receivers. ***FY 2011 Plans:*** - Develop complete brassboard A-to-I receivers and demonstrate against realistic and challenging RF environments in simulator, chamber, and/or flight tests. - Compare bandwidth, resolution, dynamic range, and power-consumption of prototype A-to-I receivers against state-of-the-art conventional receivers performing similar functions.	13.110	14.429	14.500

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
- Initiate design of direct-digital to high-power RF transmitter modules with high linearity, wide bandwidth and efficiency, focusing on reduction of electronic fratricide. ***FY 2012 Plans:*** - Develop and demonstrate through analysis, simulation and measurement feasible Look-Through transmitter architectures. - Design, tape out and characterize suitable Look-Through transmitter cells and signal combining structures.			
Title: Advanced Wide FOV Architectures for Image Reconstruction & Exploitation (AWARE) ***Description:*** The Advanced Wide FOV Architectures for Image Reconstruction & Exploitation (AWARE) program primarily addresses the passive imaging needs for multi-band, wide field of view (FOV) and high-resolution imaging for ground and near ground platforms. The AWARE program aims to solve the technological barriers that will enable FOV, high resolution and multi-band camera architectures by focusing on four major tasks: high space-bandwidth product (SBP) camera architecture; small pitch pixel focal plane array architecture; broadband focal plane array architecture; and multi-band focal plane array architecture. The AWARE program demonstrates technologies such as detectors, focal plane arrays, read-out integrated circuitry, and computational imaging that enable wide FOV and high space bandwidth, novel optical designs, high resolution and multiple wavelength band imagers. These technologies will be integrated into subsystem demonstrations under the related MT-15 project in PE 0603739E. This program also includes technologies previously addressed in the MultiScale Optical Sensor Array Imaging (MOSAIC) program. ***FY 2011 Plans:*** - Develop components to construct baseline visible wavelength camera and simulate data acquisition. - Design and fabricate visible wavelength optical system. - Complete broadband detector array test chips. - Demonstrate 10x10 LWIR 5 micron pixel pitch and complete 256x256 array design with small pitch ROIC. - Demonstrate and test hybridization schemes. ***FY 2012 Plans:*** - Demonstrate optical, electronic and software components for integrated macrocameras. - Finalize design, fabrication process and assembly of hardware for camera. - Demonstrate various operating modes with highly developed interface.	-	12.000	10.000
Title: Advanced X-Ray Integrated Sources (AXIS)	-	-	4.500

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
Description: The objective of the Advanced X-Ray Integrated Sources (AXIS) program is to greatly reduce the size, weight and power of X-ray sources while dramatically increasing their electrical efficiency through application of microscale engineering technologies such as MEMS and NEMS. Such imaging modalities should speed reverse engineering of integrated circuits to validate trustworthiness as well as contrast-free battlefield imaging of blood vessel injuries in blunt trauma. The Advanced Research component of this effort will focus on applying basic research discoveries to the development of compact, pulsed X-ray sources. Such sources are a necessary component to enable future technologies with high-speed motion imaging capabilities and the reverse engineering of integrated circuits. This program has basic research efforts funded in PE 0601101E, Project ES-01. ***FY 2012 Plans:*** - Investigate designs for compact and energy efficient X-ray sources that are spectrally tunable with narrow energy width.			
Title: Diverse & Accessible Heterogeneous Integration (DAHI) ***Description:*** Prior DARPA efforts have demonstrated the ability to monolithically integrate inherently different semiconductor types to achieve near-ideal "mix-and-match" capability for DoD circuit designers. Specifically, the Compound Semiconductor Materials On Silicon (COSMOS) program, in which transistors of Indium Phosphide (InP) can be freely mixed with Silicon Complementary Metal-Oxide Semiconductor (CMOS) circuits to obtain the benefits of both technologies (very high speed and very high circuit complexity/density, respectively). The Diverse & Accessible Heterogeneous Integration (DAHI) effort will take this capability to the next level, ultimately offering the seamless co-integration of a variety of semiconductor devices (for example, GaN, InP, GaAs, ABCS), microelectromechanical (MEMS) sensors and actuators, photonic devices (e.g., lasers, photo-detectors) and thermal management structures. This capability will revolutionize our ability to build true "systems on a chip" (SoCs) and allow dramatic size, weight and volume reductions for a wide array of system applications. In the Applied Research part of this effort, High performance RF/optoelectronic/mixed-signal SoCs for specific DoD transition applications will be developed as a demonstration of the DAHI technology. In addition, in order to provide maximum benefit to the DoD, as these processes are developed, they will be transferred to a manufacturing flow and made available (with appropriate computer aided design support) to a wide variety of DoD laboratory, FFRDC, academic and industrial designers. Manufacturing yield and reliability of the DAHI technologies will be characterized and enhanced. This program has basic research efforts funded in PE 0601101E, Project ES-01. ***FY 2012 Plans:***	-	-	10.000

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
- Optimize CMOS-compatible processes to achieve heterogeneous integration with diverse types of compound semiconductor transistors, MEMS, and non-silicon photonic devices, including interconnect and thermal management approaches. - Design high complexity heterogeneously integrated RF/optoelectronic/mixed signal and circuits, such as wide band, high-resolution analog-to-digital converters and transmitters, and optoelectronic RF signal sources. - Initiate manufacturing, yield and reliability enhancement, and multi-user foundry capability.			
Title: Microscale Plasma Devices ***Description:*** The objective of the Microscale Plasma Devices is to develop microscale plasma devices for the efficient, high pressure (up to or even including atmospheric pressure) generation of ions, radiofrequency energy, and light sources. Applications for such devices are far reaching, including the construction of complete high frequency logic circuits, and integrated circuits with superior resistance to radiation and extreme temperatures. This effort addresses the Applied Research part of the overall program, translating the basic science advances to complex circuit designs that may be integrated with commercial electronic devices. This program has basic research efforts funded in PE 0601101E, Project ES-01. ***FY 2012 Plans:*** - Demonstrate durable plasma and vacuum microelectrode structures. - Identify approaches for integration of supporting devices (e.g., thin-film photoconductors, diodes, triode vacuum devices, etc.) for complete circuit functions.	-	-	4.000
Title: Microscale Power Conversion* ***Description:*** *Formerly COmpact Power Processing Electronics Research The Microscale Power Conversion (MPC) program will address the fundamental limitations of power conversion by enabling a new technology and approach that exploits advances in basic power devices that can operate at very high frequencies with low losses. A key benefit of these new devices is that they can be integrated into very compact circuits and assemblies that will provide dramatic advances to the power bus of a platform. Specifically, this program will develop the technology to enable DC to DC power conversion for military applications at the scale of an integrated circuit so it can be embedded within the electronics subsystem and a new distributed power architecture can be realized. The focus of this program is on attaining 100MHz internal operation frequencies of power circuits since the size of the passive elements (inductors and capacitors) in a power converter scales as the fourth power of the internal operating frequency. In FY 2012 MPC moves to PE 0602715, Project MBT-03, which consolidates all of the DARPA energy programs into one project.	-	10.000	-

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
FY 2011 Plans: - Develop design and initial fabrication of critical sub-circuits and perform measurements in laboratory. - Develop theoretical design and analyses for understanding of the high-frequency trade-off space of relevant circuit designs and topologies. - Optimize transistor performance to include ultra-fast power switching capability. - Develop new fabrication techniques for incorporating high frequency transistors and devices compatible with integrated power amplifier topologies. - Document measurements of converter efficiency and losses.			
Title: Carbon Electronics for RF Applications (CERA) ***Description:*** The Carbon Electronics for RF Applications (CERA) program will develop a wafer-scale graphene (2-D carbon monolayer) synthesis process resulting in films with excellent mobility, uniformity and layer control (down to single monolayer films). These carbon films will then be used to develop ultra-low power, high-speed field effect transistors optimized for RF-applications (RF-FET). The program will conclude with a demonstration of a low power, low noise amplifier (LNA) using graphene-field effect transistors (FETs) as the channel material. ***FY 2010 Accomplishments:*** - Optimized synthesis process for wafer-scale graphene thin films. - Optimized RF-FETs based on graphene channels. ***FY 2011 Plans:*** - Increase area of graphene synthesis to wafer-scale dimensions. - Demonstrate film thickness control down to single monolayer. - Demonstrate low power, high performance RF-FETs with graphene. - Demonstrate initial wide-band LNA using graphene channel based RF-FETs.	8.764	6.958	-
Title: Leading Edge Access Program (LEAP) ***Description:*** The focus of the Leading Edge Access Program (LEAP) is to enable university, industry, and government lab access to on-shore state of the art Complementary Metal-Oxide Semiconductor (CMOS) technology for the purpose of performing advanced integrated circuit (IC) research of benefit to the DoD. Specifically, LEAP intends to offer foundry access at a substantially reduced cost for CMOS technology nodes of 45 nanometers (nm) and below. Currently much of the IC design work performed using advanced technology nodes, including that done for the DoD, uses off-shore facilities in Asia and Europe. This results in substantial intellectual property (IP) development outside the U.S. and creates a number of difficulties for technology transition of DoD-critical applications. This program will stimulate U.S.-based advanced design research, providing top	2.928	3.210	-

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
researchers early and partially subsidized access to validate and test innovative ideas and facilitate a more natural transition of pioneering ideas. ***FY 2010 Accomplishments:*** - Initiated transition of 45 nm Si On Insulator (SOI) to 32 nm bulk CMOS. ***FY 2011 Plans:*** - Transition to 32 nm SOI, 22 nm bulk CMOS, and 22 nm SOI.			
Title: Quantum Sensors ***Description:*** The Quantum Sensors program exploits non-classical effects to improve the resolution and range of military sensors. The objective of the program is to enhance sensitivity, resolution, and effectiveness of electromagnetic sensors beyond what is classically possible. In the initial effort, the types of sensors that propagate entangled light out to and back from a target were proven to be ineffective when realistic scattering and absorption occur between the source and the target. Sensors that propagate classical light to the target but use non-classical effects only in the receiver were shown to provide qualitative advantages over their classical counterparts. These include compensation for soft aperture losses using squeezed vacuum injection and compensation for detectors' quantum inefficiency using noiseless amplification. ***FY 2010 Accomplishments:*** - Designed laser radar with combined squeezed vacuum injection and noiseless amplification. ***FY 2011 Plans:*** - Test and demonstrate system performance. - Make technology available to the Services for further development.	5.089	7.639	-
Title: Spin Torque Transfer-Random Access Memory (STT-RAM) ***Description:*** The Spin Torque Transfer-Random Access Memory (STT-RAM) program will develop materials and processes to fully exploit the spin-torque transfer (STT) phenomenon for creating "universal" memory elements. This program will develop the core technology for exploiting spin-torque transfer and related phenomena for producing large-scale memories. Compatibility and stability with expected mainstream processes for semiconductor electronics and patterned media is an important attribute that should enable significant leverage for these new technologies in delivering early demonstrations and in gaining wider acceptance. ***FY 2010 Accomplishments:*** - Developed magnetic materials and architectures that allow for fast, low power switching in a STT architecture.	8.277	6.065	-

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
- Demonstrated fast low power STT memory cell that has size and endurance similar to current non-volatile electronic memories. ***FY 2011 Plans:*** - Develop improved magnetic materials that allow for faster and lower power switching in the STT architecture. - Develop processes and circuit designs to manufacture operational memory arrays in high yield.			
Title: Radio Frequency Photonics Technology (RPT) ***Description:*** The Radio Frequency Photonics Technology (RPT) program is developing components and microsystems to revolutionize deployed signal intelligence (SIGINT) gathering capabilities. The radio frequency (RF) spectrum contains innumerable friendly and adversarial signals of interest including: voice and data communications, electronic signatures, and navigation information. Conventional electronic systems are challenged in detecting weak signals in the presence of strong ones (low-linearity) across a broad range of frequencies (narrow-band). The RPT program aims to efficiently capture all RF signals of interest by developing broad-band (>10 gigahertz) high-linearity (>70 decibels dynamic-range) optical components and microsystems. RPT enables linear broadband microsystems such as remote links, channelizers, and analog-to-digital converters (ADCs). The RPT program will reduce susceptibility to electronic attack, increase the probability-of-intercepting (POI) adversaries on their first-pulse transmission, and increase information awareness 1000-fold. The Applied Research portion of this program will develop linear broadband optical components such as modulators, photodetectors, lasers, delay elements, and low-noise oscillators in support of linear broadband microsystems. These components will be integrated into subsystem demonstrations in the related RPT, PE 0603739E, Project MT-15. This program includes technologies previously addressed in the Remoted Analog-to-Digital Converter with De-serialization and Reconstruction (RADER) and Integrated Photonic Delays (iPhoD) programs. ***FY 2010 Accomplishments:*** - Refined waveguide materials, fabrication and coupling approaches. - Demonstrated a precise and low loss fiber input/output coupling technology. - Developed an analog to digital converter performance multiplier architecture. ***FY 2011 Plans:*** - Develop high-linearity photodetectors and modulators. - Demonstrate low-loss integrated optical delay lines (<0.1 decibels per meter). - Improve waveguide materials, processes, and devices to the performance levels needed for successful demonstration of an array processor.	5.300	18.129	-

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
- Fabricate an array processor with 500 ns of on-chip optical delay for the longest path.			
Title: Ultrabeam ***Description:*** The goal of the Ultrabeam program was to demonstrate the world's first gamma-ray laser using laboratory equipment. Compact gamma ray lasers can enable the development of new and more effective radiation therapies and radiation diagnostic tools for medical and materials/device inspection applications. This unique X-ray laser technology could also eventually enable the development of compact, laboratory-scale high-brightness coherent sources for 3-D molecular scale imaging of living cells and debris-free advanced lithography. ***FY 2010 Accomplishments:*** - Demonstrated 50 micro joule, 60 as X-ray laser. - Modeled gamma-ray gain of 100 per cm. ***FY 2011 Plans:*** - Demonstrate gamma-ray excitation and coherent gamma-ray amplification in solids.	1.000	2.656	-
Title: Chip-to-Chip Optical Interconnects (C2OI) ***Description:*** The performance of electronic interconnect technologies, particularly for implementing high-speed communications channels on printed circuit boards and back planes, is currently being outpaced by the ever-advancing needs of Complimentary Metal-Oxide Semiconductor (CMOS) microprocessor chips. This performance gap in the on-chip and between chip interconnection technology will create substantial data throughput bottlenecks, deleteriously affecting future military-critical sensor signal processing systems. To address this pressing issue, the Chip-to-Chip Optical Interconnects (C2OI) program is developing optical technology for implementing chip-to-chip interconnects at the board and backplane level. ***FY 2010 Accomplishments:*** - Demonstrated a chip-scale opt-electronic transceiver circuit based on C2OI operating at 1 Terabit per second (consisting of twenty four bidirectional channels each operating at 20 Gigabits/second). ***FY 2011 Plans:*** - Demonstrate a full system-scale demonstration of C2OI technology through the optical interconnect of two high performance computer servers using embedded C2OI technology integrated with commercial circuit boards.	2.000	2.321	-
Title: Near-Junction Transport (NJT) ***Description:*** The Near-Junction Transport (NJT) program explores heat conduction and mitigation through materials layers near a high-power device junction. This program will develop and verify accurate quantitative models for heat generation and transport in	-	6.089	-

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
and near device junctions to include development of novel high spatial and temporal resolution metrology techniques, fabrication of device-compatible materials and interfaces expected to offer unique thermal characteristics resulting in the development of models, tools, and materials for near-junction thermal management in a broad class of electronic device materials. The second stage will concentrate on development of specific materials to enhance the local heat-spreading in the region of the semiconductor chip. Industry leaders with the expertise in developing high-power semiconductor devices will be expected to demonstrate significantly enhanced heat density and the use of enhanced heat spreading technologies within an existing fabrication process. Additionally, the program will address developing novel device-scale structures to enable highly conductive thermal paths to remove unwanted heat from electronic devices. The impressive improvements obtained through miniaturization and integration in electronics have led to a thermal bottleneck where dense logic circuits, mixed-signal analog and digital circuits, and RF electronics are all limited by energy dissipation in small volumes. This program is a companion program to the Thermal Management Technologies (TMT) program in PE 0603739E, Project MT-12. ***FY 2011 Plans:*** - Develop specific materials to enhance the local heat-spreading in the region. - Preliminary design of thermally enhanced semiconductor device. - Demonstrate the use of enhanced heat spreading technologies within an existing fabrication process. - Demonstrate significantly enhanced heat density utilizing high-power semiconductor devices. - Identify nanostructured material designs for revolutionary thermal pathways compatible with electronic devices. - Explore the potential improvement possible by the use of phonon engineering. - Transit resulting advancements to TMT research in MT-12.			
Title: Advanced Microsystems Technology ***Description:*** The Advanced Microsystems Technology program explored a range of advanced microsystem concepts well beyond existing current technologies. The program focus was on technologies that exploit 3-D structures, new materials for Geiger-mode detectors, advance patterning, and extreme scaling in silicon devices. Insights derived in these areas will be exploited in future program initiatives. ***FY 2010 Accomplishments:*** - Developed and demonstrated a process of controllable release and handling of fiber-like silicon-on-insulator flexible electronics. - Designed and fabricated slab-coupled optical waveguide (SCOW) photodiode packages with fiber-pigtail input and microwave output. - Demonstrated successful actuation of polydimethylsiloxane (PDMS) valves for use in electowetted microfluidic devices.	5.000	-	-
Title: High Frequency Wide Band Gap Semiconductor	4.646	-	-

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
Description: The High Frequency Wide Band Gap Semiconductor program fully exploited the properties of wide bandgap semiconductors (WBGS) to enhance the capabilities of microwave and millimeter-wave (MMW) monolithic integrated circuits (MMICs) and in turn, enable future RF sensor, communication, and multifunction military capabilities. Wide bandgap semiconductors have the ability to deliver very high power and other very favorable high frequency characteristics. Prior efforts have focused on improvements to the basic semiconductor while current efforts are focused on realizing devices and circuits. These technologies will lead to affordable, high performance, reliable, wide bandgap devices and MMICs with characteristics suitable for enabling new DoD systems and greatly improved performance for fielded platforms. This effort addressed the Applied Research portion of the program. In this effort, the electronic devices with long lifetimes were developed. The effort develops models to predict device electronic performance and reliability characteristics, to ensure reproducible behavior and to enable integration of these devices into integrated circuits. This program also has efforts funded in PE 0603739E, project MT-15. ***FY 2010 Accomplishments:*** - Developed and utilized physics-based models that accurately predict device performance. - Demonstrated reproducible WBGS device and MMICs fabrication processes. - Demonstrated WBGS devices and MMICs that, while maintaining high levels of producibility and reliability, achieved substantially higher levels of performance compared to GaAs-based microwave and MMW devices and MMICs.			
Title: Parametric Optical Processes and Systems (POPS) ***Description:*** The Parametric Optical Processes and Systems (POPS) program has demonstrated all optical signal processing based on Four Wave Mixing in optical fibers and using silicon waveguides to achieve data rates of 100 Gigabits per second (Gb/s) to 1 Terabit per second (Tb/s). This program developed components such as wavelength-shifting wideband amplifiers, tunable optical delays, and parametric sampling for this application. These components will be used in higher level sub-systems such as serializers, de-serializers, and wavelength grooming devices at high data rates of 100 Gb/s - 1Tb/s. These demonstrations of functionality also included quantitative bit error rate measurements. POPS components and subsystems will enable optical communications at data rates ten times higher than currently possible with conventional approaches. POPS technology will allow all optical manipulation of high rate data streams with a precision and flexibility not currently possible. ***FY 2010 Accomplishments:*** - Demonstrated enhanced serializer component with data rate of 640 Gb/s. - Demonstrated enhanced deserializer component with granularity of 10 Gb/s.	3.577	-	-

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C. Accomplishments/Planned Programs ($ in Millions)	FY 2010	FY 2011	FY 2012
- Demonstrated 3000 nano second continuous parametric delay technology.			
Title: Semiconductor-Tuned HTS Filters for Ultra-Sensitive RF Receivers (SURF) ***Description:*** The Semiconductor-Tuned HTS Filters for Ultra-Sensitive RF Receivers (SURF) program increased the tuning speed of high-temperature semiconducting (HTS) filters, from about a second with present mechanical methods, to microsecond speeds required for systems such as the Joint Tactical Information Distribution System (JTIDS). The technology for such a million-fold improvement relied upon semiconductor tuning, properly mated with the superconducting filter materials; the fundamental challenge - that normal electrical conductivity and superconductivity cannot coexist in the same circuit - has been overcome. In addition to interference-rejection at microsecond speeds, these filters make it possible to perform wide spectral searches with unprecedented frequency resolution, enabling detection of very weak emissions (signatures) characteristic of threat systems. Such a capability within a small add-on box to the RF receiver revolutionized the performance of all types of receivers, with applications ranging from communications to signals intelligence, and enabled operation in the densest of interference environments. ***FY 2010 Accomplishments:*** - Developed a concept for a front-end pre-selector filter bank, consisting of both tunable notch and bandpass filters, which demonstrated the capability of removing local interference, particular those agile signals such as JTIDS. - Constructed a pre-selector module, incorporating HTS filters and supporting circuitry, and demonstrated the capability of eliminating interference in the first stage of the receiver.	1.298	-	-
Accomplishments/Planned Programs Subtotals	182.188	286.936	215.178

	FY 2010	FY 2011
Congressional Add: 3-D Technology for Advanced Sensor Systems ***FY 2010 Accomplishments:*** - Continued 3-D device development.	2.000	-
Congressional Adds Subtotals	2.000	-

D. Other Program Funding Summary ($ in Millions)

N/A

E. Acquisition Strategy

N/A

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F. Performance Metrics

Specific programmatic performance metrics are listed above in the program accomplishments and plans section.