RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, Project ELT-01

COST (In Millions)	FY 2007	FY 2008	FY 2009	FY 2010	FY 2011	FY 2012	FY 2013
Total Program Element (PE) Cost	215.742	196.707	211.457	229.195	237.767	238.162	248.066
Electronics Technology ELT-01	215.742	196.707	211.457	229.195	237.767	238.162	248.066

(U)   Mission Description:

(U)   This program element is budgeted in the Applied Research budget activity because its objective is to develop electronics that make a wide range of military applications possible.

(U)   Advances in microelectronic device technologies, including digital, analog, photonic and microelectromechanical systems (MEMS) devices, continue to have significant impact in support of defense technologies for improved weapons effectiveness, improved intelligence capabilities and enhanced information superiority. The Electronics Technology program element supports the continued advancement of these technologies through the development of performance driven advanced capabilities, exceeding that available through commercial sources, in electronic, optoelectronic and MEMS devices, semiconductor device design and fabrication techniques, and new materials and material structures for device applications. A particular focus for this work is the exploitation of chip-scale heterogeneous integration technologies that permit the optimization of device and integrated module performance.

(U)   The phenomenal progress in current electronics and computer chips will face the fundamental limits of silicon technology in the early 21st century, a barrier that must be overcome in order for progress to continue. Another thrust of the program element will explore alternatives to silicon-based electronics in the areas of new electronic devices, new architectures to use them, new software to program the systems, and new methods to fabricate the chips. Approaches include nanotechnology, nanoelectronics, molecular electronics, spin-based electronics, quantum-computing, new circuit architectures optimizing these new devices, and new computer and electronic systems architectures. Projects will investigate the feasibility, design, and development of powerful information technology devices and systems using approaches to electronic device designs that extend beyond traditional Complementary Metal Oxide Semiconductor (CMOS) scaling, including non silicon-based materials technologies, to achieve low cost, reliable, fast and secure computing, communication, and storage systems. This investigation is aimed at developing new capabilities from promising directions in the design of information processing components using both inorganic and organic substrates, designs of components and systems leveraging quantum effects and chaos, and innovative approaches to computing designs

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

incorporating these components for such applications as low cost seamless pervasive computing, ultra-fast computing, and sensing and actuation devices. This project has five major thrusts:

- Electronics: The manipulation of electrons in digital, analog, and mixed signal circuits for sensing, processing, and communications. This thrust includes such programs as Advanced Microsystems Technology Program; Applications of Molecular Electronics (MoleApps); High Frequency Wide Band Gap Semiconductor Electronics Technology; High Power Wide Band Gap Semiconductor Electronics Technology; J-Band Advance Digital Receiver (JADR); Ideal Channel Electronics (ICE); Quantum Information Science (QIS); Robust Integrated Power Electronics (RIPE); Submillimeter Wave Imaging FPA Technology (SWIFT); Technology Efficient Agile Mixed Signal Microsystem (TEAM); Technology for Frequency Agile Digitally Synthesized Transmitters (TFAST); Feedback-Linearized Microwave Amplifiers; Terahertz Imaging Focal-Plane Technology (TIFT); Trusted, Uncompromised Semiconductor Technology (TrUST); Carbon Electronics for RF Applications (CERA); Compound Semiconductor Materials On Silicon (COSMOS); Compact Vacuum Electronic Radio Frequency Technology (COVERT (HiFIVE)); Steep-subthreshold-slope Transistors for Electronics with Extremely-low Power (STEEP); Semiconductor-Tuned HTS Filters for Ultra-Sensitive RF Receivers (SURF); Thz Transistors; and Ultra-low Power Subthreshold Electronics (UPSE).

- Photonics: The generation, detection, and modulation of photons for imaging, communications, and sensing. This thrust encompasses the following programs: Adaptive Focal Plane Arrays (AFPA); Advanced Precision Optical Oscillator (APROPOS); Bio-Electronics and Photonics; Chip-to-Chip Optical Interconnects; Photonic Analog Signal Processing Engines with Reconfigurability (PhASER); Parametric Optical Processes and Systems (POPS); Linear Photonic radio frequency (RF) Front End Technology (PHOR-FRONT); Optical Arbitrary Waveform Generation (OAWG); Transparent Displays; Systems of Neuromorphic Adaptive Plastic Scalable Electronics (SyNAPSE); Technology for Agile Coherent Optical Transmission & Signal Processing (TACOTA); Ultrabeam; Photonic Bandwidth Compression for Instaneous WideBand Analog to Digital (A/D) Conversion; Novel Technologies for Optoelectronics Materials Manufacturing (NTOMM); Optical Antenna Based on Nanowires; Short Range Wide-field-of-regard Extremely-agile Electronically-Steered Photonic Emitter & Receiver (SWEEPER); Ultra Low Loss Photonic Integrated Circuits and Processors; Visible InGan Injection Lasers (VIGIL); Ultra Fast Lasers with Response > 100 GHz; Precision OptoMechanics – Mechanical Properties of light; Raman Beam Combining and Cleanup; Frequency Domain Analog Optical Signal Processor; Receiver Power Optimized for Reconnaissance and Tagging (REPORT); Non-Contact EEG Technologies (NET); and Ultra-low Power Subthreshold Electronics.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, Project ELT-01

- MicroElectroMechancial Systems (MEMS): Exploitation of the processing tools and materials from semiconductor technology to build electro-mechanical structures at the micro- and nano-scale. The MEMS thrust encompasses: 3-D Microelectromagentic RF Systems (3-D MERFS); Chip Scale Atomic Clock; Radioisotope Micropower Sources (RIMS); and Micro Isotope Micro-Power Sources (MIPS).

- Architectures: Exploitation of new arrangements of materials, devices, and circuits to increase performance or reduce power. Programs under this thrust include: Analog-to-Information (A-to-I); Computational Imaging (CI); Design Tools for 3-Dimensional Electronic Circuit Integration; Multiple Optical Non-Redundant Aperture Generalized Sensors (MONTAGE); Polymorphous Computing Architecture (PCA); Vertically Interconnected Sensor Arrays (VISA); and Structured ASIC Design (StASD).

- Algorithms: Exploitation of insights into mathematical constructs for data representation, process control, and discrimination routines by leveraging knowledge of Microsystem hardware operation. Programs under this thrust include: Cognitively Augmented Design for Quantum Technology (CAD-QT); Design-space Exploration and Synthesis Technology for Integrating nontraditional Microsystems at yield (DESTINY); Non-Linear Math for Mixed Signal Microsystems; Processing Algorithms with Co-design of Electronics (PACE); and Quantum Sensors.

- Other Electronic Technology Research: National Secure Foundry Initiative; Characterization, Reliability and Applications for 3-D Microdevices; and 3-D Technology for Advance Sensor Systems.

(U) <u>**Program Accomplishments/Planned Programs:**</u>

	FY 2007	FY 2008	FY 2009
Advanced Microsystems Technology Program	5.000	5.000	5.000

(U)   The Advanced Microsystems Technology program will explore a range of advanced microsystem concepts well beyond existing current technologies. The program focuses on technologies that exploit 3-dimensional (3-D) structures, new materials for Gieger mode detectors, advance patterning, and extreme scaling in silicon devices. Insights derived in these areas will be exploited in future program initiatives. These initiatives include advanced high-resolution lithography, high speed avalanche devices with response out to 2 micrometers (um); integration of periodic elements III-V material with silicon; and novel cryogenic electronics.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	**DATE** February 2008
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

(U)   Program Plans:
FY 2007 Accomplishments:
−   Established and exercised multi-project wafer runs for 3-D integrated circuits.
−   Demonstrated bonding and functionality of Silicon-On-Insulator circuits to Indium Phosphide detectors.
−   Extended maskless multiple exposure system to 2x smaller features.
FY 2008 Plans:
−   Demonstrate photoresist capable of multiple in-situ exposure with enhanced resolution.
−   Demonstrate sub-35 nanometer (nm) half-pitch interometric liquid exposure capability.
FY 2009 Plans:
−   Prepare report analyzing prospects for beyond roadmap technologies.
−   Deliver data on ultra-low voltage operation of Silicon CMOS for DoD applications.

	FY 2007	FY 2008	FY 2009
Applications of Molecular Electronics (MoleApps)	3.638	0.000	0.000

(U)   The goal of the Applications of Molecular Electronics (MoleApps) program extended the capabilities being developed in the previous Moletronics program to demonstrate the computational processing capabilities of molecular electronics in a system that integrates memory with control logic and data paths. This approach allowed the use of simpler processor designs to demonstrate the advantages of nano-scale molecular electronics that do not have the conventional circuitry overhead associated with modern pipeline chip designs.

(U)   Program Plans:
FY 2007 Accomplishments:
−   Constructed combinatorial logic functions assembled from molecular-scale components.
−   Demonstrated molecular electronics sensor array capable of probability of detection > 0.95 and false positive < 0.01.
−   Demonstrated sequential logic, control and Input/Output (I/O) circuit compatible with memory and full computer design.

			DATE	
RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)			February 2008	

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

	FY 2007	FY 2008	FY 2009
High Frequency Wide Band Gap Semiconductor Electronics Technology	30.711	25.000	25.000

(U)   The High Frequency Wide Band Gap Semiconductor Electronics Technology program is developing high performance, cost-effective high-power electronic devices that exploit the unique properties of wide band gap semiconductors. Specifically, this program will develop low defect epitaxial films, high yield fabrication processes, and device structures for integrated electronic devices for emitting and detecting high-power radio frequency/microwave radiation, and high power delivery and control.

(U)   Program Plans:
  FY 2007 Accomplishments:
  – Developed bulk and surface process technologies for reducing or mitigating crystallographic defects in wide bandgap materials.
  – Developed semi-insulating substrates for high frequency devices.
  – Designed high power enclosures for microwave electronic assemblies.
  – Demonstrated large periphery high power devices suitable for microwave and mm-wave operation.
  – Demonstrated process reproducibility and minimization of yield limiting factors.
  – Established device characterization for very high power solid-state amplifiers.
  – Demonstrated 100 mm Silicon Carbide (SiC) and wide band gap alternate substrates with less than 80 micropipe/cm^2 and resistivity 10^6 ohms-cm.
  FY 2008 Plans:
  – Demonstrate epitaxial processes that yield + 3% uniformity over 75 mm wide bandgap substrates.
  – Initiate thermal management study to determine best packaging approach for high power, high frequency microwave and millimeter wave transistors.
  – Demonstrate 100 mm SiC and wide band gap alternate substrates with less than 40 micropipe/cm^2 and resistivity 10^7 ohms-cm.
  – Demonstrate epitaxial processes that yield + 1% uniformity over 100 mm wide bandgap substrates.
  – Identify fabrication processes for robust microwave and mm-wave devices.
  FY 2009 Plans:
  – Identify thermal management concepts to sustain more than 1 KW/cm^2 power density in high-power devices.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	**DATE** February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

– Optimize wide bandgap semiconductor materials to achieve 100 mm substrates with less than 10 micropipe/cm^2 and resistivity greater than 10^7 ohms-cm at room temperature.
– Demonstrate fabrication processes for robust microwave and mm-wave devices with radio frequency yields greater than 70 percent.
– Demonstrate thermal management concepts to sustain more than 1KW/cm^2 power density in high power device.

	FY 2007	FY 2008	FY 2009
High Power Wide Band Gap Semiconductor Electronics Technology	10.500	1.500	1.000

(U)   An initiative in High Power Wide Band Gap Semiconductor Electronics Technology will develop components and electronic integration technologies for high power, high frequency microsystem applications based on wide bandgap semiconductors.

(U)   Program Plans:
FY 2007 Accomplishments:
– Developed low defect conducting Silicon Carbide (SiC) substrate consistent with yielding 1 cm^2 devices.
– Developed lightly doped, thick (more than 100 micron) SiC epitaxy with low defects to enable 10 kV class power devices.
– Developed low on-state resistance SiC diodes capable of blocking 10 kV.
– Demonstrated SiC wafer and thick epitaxy with less than 1.5 catastrophic defects per cm^2 consistent with 10 kV reverse blocking.
– Initiated work on Megawatt class SiC power device able to switch at more then 100 kHz.
– Initiated work on packaging of high power density, high temperature SiC power electronics.
FY 2008 Plans:
– Demonstrate megawatt Class SiC power devices.
– Demonstrate high power density packaging for greater than 10 kV operations.
FY 2009 Plans:
– Develop integrated power control logic compatible with high temperature and power SiC power devices.

		DATE	
RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)		February 2008	

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

	FY 2007	FY 2008	FY 2009
Quantum Information Science (QIS)	8.240	4.240	3.350

(U)   The Quantum Information Science (QIS) program will explore all facets of the research necessary to create new technologies based on quantum information science. Research in this area has the ultimate goal of demonstrating the potentially significant advantages of quantum mechanical effects in communication and computing. Expected applications include: new improved forms of highly secure communication; faster algorithms for optimization in logistics and wargaming; highly precise measurements of time and position on the earth and in space; and new image and signal processing methods for target tracking. Technical challenges include: loss of information due to quantum decoherence; limited communication distance due to signal attenuation; limited selection of algorithms and protocols; and larger numbers of bits. Error correction codes, fault tolerant schemes, and longer decoherence times will address the loss of information. Signal attenuation will be overcome by exploiting quantum repeaters. New algorithm techniques and complexity analysis will increase the selection of algorithms, as will a focus on signal processing. The QIS program is a broad-based effort that will continue to explore the fundamental open questions, the discovery of novel algorithms, and the theoretical and experimental limitations of quantum processing as well as the construction of efficient implementations.

(U)   Program Plans:
FY 2007 Accomplishments:
− Refined quantum architecture and designed solutions for problems such as graph isomorphism, imaging, and signal processing.
− Investigated alternative protocols for secure quantum communication, quantum complexity, and control.
− Integrated improved single and entangled photon sources and detectors into existing quantum communication networks.
FY 2008 Plans:
− Investigate alternative designs, architectures and devices for quantum communication and demonstrate high-rate (1Gbit/sec) quantum-secure communication over a single link.
FY 2009 Plans:
− Investigate unresolved fundamental issues related to quantum information science.
− Employ qubit architectures to demonstrate an application of interest to the DoD (e.g., quantum repeater, secure metropolitan-area network).
− Demonstrate interoperation between multiple qubit types to interconnect quantum communications links.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)		**DATE** February 2008	

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

	FY 2007	FY 2008	FY 2009
Robust Integrated Power Electronics (RIPE)	8.879	5.753	4.800

(U)   The Robust Integrated Power Electronics (RIPE) program will develop new semiconductor materials, devices, and circuits that enable highly compact, highly efficient electronic power converter modules. These new modules will be capable of providing up to 50kW of power per module at a power density of 500W/cubic inch. Based on fundamental material properties, the new power modules will be capable of operating in harsh environments. These new power converters will reduce the launch weight of space-based platforms by hundreds of pounds and will enable new modes of operation where the power conversion is done at the point of load and provides high quality power to payloads. Application of RIPE on Naval surface ships would result in a significant reduction of power supply weight; allowing for additional electronic components and/or weapons.

(U)   Program Plans:
   FY 2007 Accomplishments:
   −   Identified key technical challenges and quantified impact on potential platforms.
   FY 2008 Plans:
   −   Perform concept study to define opportunities for smart power and the potential for integrating silicon carbide, or other wide band gap semiconductor, with silicon electronics.
   −   Select and optimize wide band gap materials and processes for smart power circuits.
   FY 2009 Plans:
   −   Develop integration techniques for silicon carbide, or other wide bandgap semiconductor, onto silicon and/or silicon onto silicon carbide.
   −   Develop low on-resistance, fast switching silicon carbide power devices with hybrid control electronics.

<table>
<tr><td colspan="2">**RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)**</td><td>**DATE**
February 2008</td></tr>
<tr><td>**APPROPRIATION/BUDGET ACTIVITY**
RDT&E, Defense-wide
BA2 Applied Research</td><td colspan="2">**R-1 ITEM NOMENCLATURE**
Electronics Technology
PE 0602716E, Project ELT-01</td></tr>
</table>

	FY 2007	FY 2008	FY 2009
Submillimeter Wave Imaging Focal Plane Array (FPA) Technology (SWIFT)	5.116	5.260	0.000

(U)   The Submillimeter Wave Imaging Focal Plane Array (FPA) Technology (SWIFT) program will develop revolutionary component and integration technologies to enable exploitation of this spectral region. A specific objective will be the development of a new class of sensors capable of low-power, video-rate, background and diffraction limited submillimeter imaging.

(U)   Program Plans:
   FY 2007 Accomplishments:
   −   Developed compact, efficient, and high-power THz (terahertz) sources using new electronic and frequency conversion approaches.
   FY 2008 Plans:
   −   Develop sensitive and large format receiver arrays, advanced integration, and backend signal processing techniques.
   −   Develop and demonstrate a submillimeter focal plane imager.

	FY 2007	FY 2008	FY 2009
Technology Efficient, Agile Mixed Signal Microsystem (TEAM)	5.254	0.000	0.000

(U)   Technology for Efficient, Agile Mixed Signal Microsystems (TEAM) explored fabrication of high performance mixed signal systems-on-chip that will be the core of the embedded electronics in new platforms that are constrained by size and on-board power.

(U)   Program Plans:
   FY 2007 Accomplishments:
   −   Demonstrated several large-scale compelling radio frequency (RF)-technology integrated circuits (ICs):
      --   60 GHz (gigahertz) transceiver.
      --   Radar-on-a-chip front end demo (7 – 18 GHz).
      --   Electronic warfare receiver (2-18 GHz).

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, Project ELT-01

− Developed enhanced passive components for silicon-germanium (SiGe) RF technology.

	FY 2007	FY 2008	FY 2009
Technology for Frequency Agile Digitally Synthesized Transmitters (TFAST)	8.120	7.420	0.000

(U)   The Technology for Frequency Agile Digitally Synthesized Transmitters (TFAST) program (Ultra High-Speed Circuit Technology) will develop super-scaled Indium Phosphide (InP) Heterojunction Bipolar Transistor (HBT) technology compatible with a ten-fold increase in transistor integration for complex mixed signal circuits. Phase I established the core transistor and circuit technology to enable the demonstration of critical small scale circuit building blocks suitable for complex mixed signal circuits operating at speeds three times that currently achievable and ten times lower power. Phase II is extending the technology to the demonstration of complex (more than 20,000 transistors) mixed signal circuits with an emphasis on direct digital synthesizers for frequency agile transmitters.

(U)   Program Plans:
FY 2007 Accomplishments:
− Developed material and processed technology for super-scaled InP double heterostructure bipolar transistors (DHBTs).
− Extended the core DHBT and interconnect technology with the implementation of complex mixed signal circuits.
− Developed super-scaled InP HBT processing technology for 0.25 micron and below.
− Developed greater than 100 gigahertz (GHz) mixed signal circuit building blocks.
− Demonstrated a critical mixed signal building block circuit operating at more than 100 GHz.
− Developed circuit designs for direct digital frequency synthesizers (DDS) operating with clock speed up to 30 GHz.
− Demonstrated world's fastest transistor, frequency divider, and mixed signal circuit.
FY 2008 Plans:
− Develop full circuit capability using super-scaled InP HBTs in complex (more than 20,000 transistor) circuits.
− Establish device models and critical design rules.
− Continue further development of world's fastest InP HBT device technology.

	DATE
RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

	FY 2007	FY 2008	FY 2009
Feedback-Linearized Microwave Amplifiers	5.580	4.970	3.840

(U)   Modern military platforms are requiring increased dynamic range receivers for their onboard communications, in both radar and electronic warfare antenna systems. The goal of the Feedback-Linearized Microwave Amplifiers program is to develop radio frequency (RF) amplifiers with revolutionary increased dynamic range receivers through the use of linear negative feedback. This program will develop the core technologies and components that may be used as building blocks and/or modules in future system applications. This program will leverage technologies from the TFAST program.

(U)   Program Plans:
FY 2007 Accomplishments:
–   Demonstrated record ultra-wideband high-linearity Indium Phosphide (InP) Heterojunction Bipolar Transistor (HBT)-based RF operational amplifier and record InP high electron mobility transistor (HEMT).
–   Demonstrated world's first enhancement-mode InP HEMT.
–   Demonstrated ultra-high linearity RF amplifiers.
FY 2008 Plans:
–   Develop InP HBT-based ultra-high linearity low-noise amplifier circuit architecture and develop low-noise InP HEMT devices.
FY 2009 Plans:
–   Develop and enhance InP HBT-based RF operational amplifier and InP HEMT-based ultra-low-noise amplifier.

	FY 2007	FY 2008	FY 2009
Terahertz Imaging Focal-Plane Technology (TIFT)	10.667	10.440	7.000

(U)   The Terahertz Imaging Focal-Plane Technology (TIFT) program will demonstrate large, multi-element (> 40K pixels) detector receiver focal plane arrays that respond to radiation in the terahertz (THz) band (> 0.557 THz). The sensor system will be able to operate effectively at a stand-off range (> 25m) with a high spatial resolution (< 2 cm) limited only by beam diffraction. The imaging receiver will produce a two-

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, Project ELT-01

dimensional image in which each pixel records the relative intensity of the THz radiation received on the focal plane within the appropriate section of the field of view of the scene being sensed. The program will achieve intensity sensitivities as close as possible to the thermal background limit at room temperature. The minimal acceptable acquisition time is video-rate (30 Hz (hertz)). The receiver may be either passive or active (including THz time domain methods). The size, weight, and electrical power requirements will be consistent with portability.

(U)   Program Plans:
   FY 2007 Accomplishments:
   – Demonstrated revolutionary component and integration technologies necessary for the development of a diffraction-limited, video-rate THz (at least 0.557×10^{12}Hz) frequency imager.
   FY 2008 Plans:
   – Demonstrate a compact THz source achieving at least 10 mW of average power and 1% wall plug efficiency, as required for active illumination and/or for local oscillators in heterodyne or homodyne detection schemes.
   FY 2009 Plans:
   – Demonstrate a THz receiver capable of achieving a noise equivalent power of less than 1 pW/Hz $^{1/2}$ as measured with an integrated acquisition time of no more than 30 milliseconds and a pre-detection bandwidth of no more than 50 GHz (gigahertz), as required in order to achieve a system-level noise equivalent delta temperature of 1K or better.

	FY 2007	FY 2008	FY 2009
Trusted, Uncompromised Semiconductor Technology (TrUST)	12.982	19.817	2.000

(U)   The Trusted, Uncompromised Semiconductor Technology (TrUST) program will explore techniques to insure Integrated Circuits (ICs) of interest to the DoD can be certified as trustworthy after fabrication. These efforts will compliment other maskless lithography and verifiable design programs. The first thrust will develop new tools and techniques for rapidly analyzing fabricated circuits and comparing the circuit topology to that of the design produced at the trusted design source. The second thrust will exploit emerging research in 3-dimensional (3-D) stacked and monolithic circuits to distribute, or segment, a complex IC into smaller sub-circuits. In this way, the sub-circuits can be fabricated separately, making it more difficult to compromise the complete circuit and making it easier to characterize each circuit for trustworthiness. This approach will also leverage the performance advances projected for 3-D architectures. The final thrust will explore novel ways to add a "hardware jacket" to complete IC's that will serve to monitor the circuits' performance and raise a flag if unspecified operations are encountered.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, Project ELT-01

(U)   Program Plans:

FY 2007 Accomplishments:
−   Developed new tools and techniques for rapidly analyzing fabricated circuits and comparing the circuit topology to that of the design produced at the trusted design source.
−   Exploited emerging research in 3-D stacked and monolithic circuits to distribute, or segment, a complex IC into smaller sub-circuits.

FY 2008 Plans:
−   Explore novel ways to add a "hardware jacket" to complete ICs that will serve to monitor the circuits' performance and raise a flag if unspecified operations are encountered.
−   Develop distributed circuit architectures by building trusted circuits through 3-D segmented designs.

FY 2009 Plans:
−   Explore Integrated Circuit monitoring for deployed performance verification.

	FY 2007	FY 2008	FY 2009
Carbon Electronics for RF Applications (CERA)*	0.000	4.406	5.000

*Formerly titled Co-integration of Carbon-Based RF Electronics with Silicon Technology (CrEST).

(U)   The Carbon Electronics for RF Applications (CERA) program seeks to develop metal oxide silicon field effect transistors based on the planar carbon monolayer (graphene) system. Such a system has most of the desirable properties of carbon nanotubes, but found in a planar geometry, which is much more compatible with standard Complementary Metal-Oxide Semiconductor (CMOS) processing. The 10x mobility enhancement of graphene with respect to silicon will be exploited for high performance (high current drive) and low power electronics applications. The excellent mobility is achieved in a monolayer system, which is ideal from the electrostatic (i.e., gate control) point of view enabling efficient scaling to very small device geometries. Graphene Field-Effect Transistor (FET) devices are envisioned to be an enhancement, not replacement for silicon CMOS, for critical radio frequency or mixed signal circuit elements. Thus, the demonstrated integration of graphene devices into standard silicon CMOS processing is a key task of this program.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	**DATE** February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

(U) Program Plans:
FY 2008 Plans:
− Demonstrate hybrid graphene-silicon CMOS circuits for high performance and low power applications.
FY 2009 Plans:
− Integrate graphene devices into standard silicon CMOS processing.

	FY 2007	FY 2008	FY 2009
Compound Semiconductor Materials On Silicon (COSMOS)	6.579	6.680	16.040

(U) The objective of the Compound Semiconductor Materials On Silicon (COSMOS) program will be to develop new methods to tightly integrate compound semiconductor technologies within silicon CMOS circuits in order to achieve unprecedented circuit performance levels. Currently, heterogeneous integration of compound semiconductors with silicon is typically achieved through the use of multi-chip modules and similar assemblies. While adequate for relatively low performance applications (e.g., power amplifiers for cellular telephone handsets), the integration complexity that can be achieved in this manner is extremely limited. At the other end of the spectrum, epitaxial methods to grow III-V materials onto silicon substrates have generally proven unsatisfactory due to high defect densities, cost, and inflexibility in supporting multiple technologies. Instead, COSMOS will focus on an intermediate approach, which is likely to be the most successful strategy in terms of performance, size and cost. This will involve sub-circuit integration in which III-V materials devices are placed onto a processed CMOS wafer.

(U) Program Plans:
FY 2007 Accomplishments:
− Demonstrated ultra-low power dissipation circuits.
− Investigated approaches that permit mix-and-match of devices processed either before or after placement.
− Demonstrated device placement and interconnect capabilities.
− Refined and demonstrated an approach for intimate compound semiconductor/CMOS integration.
FY 2008 Plans:
− Develop methods for sub-circuit integration onto fully processed CMOS wafers.
− Develop scalable electro-magnetic (EM), thermal and mechanical models.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, Project ELT-01

− Estimate thermal and mechanical properties of integration materials and perform thermal and stress modeling to determine and improve the viability of the COSMOS thermal and mechanical design.

FY 2009 Plans:

− Fabricate wafers using the COSMOS process.
− Evaluate alignment and bonding methods to achieve mechanical integrity of dissimilar materials, post-processing compatibility with CMOS, and the achievement of high fabrication yields.
− Extend the capabilities of wide band gap devices for use in power amplifiers (PAs) at frequencies at least as high as X-band and to make this technology useful at very high frequencies.
− Demonstrate large (>1 mm) devices.
− Decrease the number of optical phonons in the critical gate region of radio frequency (RF) PA devices.

	FY 2007	FY 2008	FY 2009
Steep-subthreshold-slope Transistors for Electronics with Extremely-low Power	0.000	8.000	8.730

(U)   The Steep-subthreshold-slope Transistors for Electronics with Extremely-low Power (STEEP) program seeks to develop field emission (tunneling) based Metal Oxide Silicon Field Effect Transistors (MOSFETs). Such devices would enable lowering supply voltages by 5x, which would result in an active power savings of 25x and a stand-by power saving of at least 5x. Prototype circuits will be developed showing such power savings with little to no impact on performance (current drive). These field emission devices will be integrated into standard CMOS based processing methods and offer significant CMOS power reduction with no performance penalty.

(U)   Program Plans:

FY 2008 Plans:

− Develop novel MOSFET switch with significantly steeper sub-threshold slope.
− Develop CMOS process integration.

FY 2009 Plans:

− Optimize drive current in presence of tunneling barrier.
− Demonstrate ultra-low power, high performance prototype circuits.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)		**DATE** February 2008	

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

	FY 2007	FY 2008	FY 2009
COmpact Vacuum Electronic Radio-frequency Technology (COVERT) (HiFIVE)	0.000	4.000	5.000

(U)   The goal of the Compact Vacuum Electronic Radio-frequency Technology (COVERT) (HiFIVE) program is to demonstrate microfabricated, integrated vacuum tubes operating at 220 gigahertz (GHz) with a minimum of 50 watts of output power and 5 GHz bandwidth. The COVERT program figure of merit will be power bandwidth product, and the goal is to achieve 500 power-bandwidth (W-GHz). The ultimate goal is to develop a micro-fabricated, high-bandwidth, high-power "upper" millimeter-wave (220 GHz) amplifier consisting of an integrated high-power amplifier (HPA) consisting of a solid-state millimeter-wave monolithic integrated circuit (MMIC) driver, an integrated cathode, compression optics, micromachined interaction structure, and beam collector.

(U)   Program Plans:
         FY 2008 Plans:
         −   Demonstrate a high aspect ratio beam with required power and transport efficiency.
         FY 2009 Plans:
         −   Validate cold test interaction of structure design and high current density cathode.

	FY 2007	FY 2008	FY 2009
Semiconductor-Tuned HTS Filters for Ultra-Sensitive RF Receivers (SURF)	0.000	4.169	3.213

(U)   The operation of frequency-hopping radios greatly interferes with co-located ultra-sensitive receivers. The situation will get worse as the "hoppers" proliferate, even interfering within the receive channels of one another. At present there is no solution to this problem, other than turning off the receivers when communicating. A general solution would be to use "brick-wall" front-end filters for the receivers, re-tuning at the rate of the hoppers, if such agile filters were available. High-temperature superconducting (HTS) filters have been used very successfully for negating strong transmissions at nearby frequencies, and are unique in their ability to totally reject out-of-band signals without attenuation of signals in the pass-band. However, they have been used only for rejection of fixed-frequency interference. The Semiconductor-Tuned HTS Filters for Ultra-Sensitive RF Receivers (SURF) program will increase the tuning speed of HTS filters, from about a second with present mechanical

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, Project ELT-01

methods, to microsecond speeds required for systems such as the Joint Tactical Information Distribution System (JTIDS). The technology for such a million-fold improvement will rely upon semiconductor tuning, properly mated with the superconducting filter materials. In addition to interference-rejection at microsecond speeds, these filters will make it possible to perform wide spectral searches with unprecedented frequency resolution, enabling detection of very weak emissions (signatures) characteristic of threat systems.

(U)   Program Plans:
FY 2008 Plans:
− Demonstrate one microsecond switching of HTS filters, between three frequencies.
− Develop models of the high-temperature superconducting (HTS) tunable filters.
− Achieve microsecond stepwise semiconductor switching between three stable states.
− Continue development of low-loss semiconductor tuning elements for HTS filters, operating at cryogenic temperatures.
− Demonstrate stepwise tuning of HTS filters at microsecond increments over a broad tuning range.
FY 2009 Plans:
− Complete the development of reconfigurable filter design tools.
− Demonstrate the operation of continuously tunable notch and passband filters, using cryo-optimized semiconductor and varactor tuning elements.

	FY 2007	FY 2008	FY 2009
Adaptive Focal Plane Arrays (AFPA)	4.000	2.870	1.275

(U)   The goal of the Adaptive Focal Plane Arrays (AFPA) program is to demonstrate high-performance focal plane arrays that are widely tunable across the entire infrared (IR) spectrum (including the short-, middle- and long-wave IR bands), thus enabling "hyperspectral imaging on a chip." This program will also allow for broadband Forward Looking Infrared (FLIR) imaging with high spatial resolution. These AFPAs will be electrically tunable on a pixel-by-pixel basis, thus enabling the real-time reconfiguration of the array to maximize either spectral coverage or spatial resolution. The AFPAs will not simply be multi-functional, but rather will be adaptable by means of electronic control at each pixel. Thus, the AFPAs will serve as an intelligent front-end to an optoelectronic microsystem. The AFPA program outcome will be a large format focal plane array that provides the best of both FLIR and Hyper-Spectral Imaging (HSI).

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, Project ELT-01

(U)   Program Plans:

FY 2007 Accomplishments:

− Developed component technology (tunable IR photodetectors).

FY 2008 Plans:

− Integrate detector array.

− Demonstrate pixel-by-pixel electrical tunability in IR.

FY 2009 Plans:

− Demonstrate AFPA prototype field using a large format array.

	FY 2007	FY 2008	FY 2009
Advanced Precision Optical Oscillator (APROPOS)	6.020	2.200	0.000

(U)   The Advanced Precision Optical Oscillator (APROPOS) program will leverage advances in materials and lasers to develop new precision microwave-stable local oscillators with extremely low phase noise (up to 50 decibels better than the current state of the art) at small offsets from microwave carrier frequencies. This capability will enhance performance of radars in the detection of slow moving targets, electronic warfare systems in the identification of specific emitters, and communication systems in weak signal detection and clutter suppression all at increased stand-off range.

(U)   Program Plans:

FY 2007 Accomplishments:

− Demonstrated first opto-electronic oscillator without any electronic radio frequency (RF) amplifier.

− Demonstrated 10 gigahertz RF Optical Oscillator that outperforms any existing RF oscillator at 1 hertz to 10 kilohertz frequency offsets.

− Demonstrated tunable Opto-Electronic Oscillator with phase noise performance 20 decibels better than best synthesizer alternative.

FY 2008 Plans:

− Develop an opto-electronic oscillator with ultra low phase noise, tunable oscillator range, and vibration sensitivity.

	DATE
RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

	FY 2007	FY 2008	FY 2009
Bio-Electronics and Photonics	4.000	5.000	0.000

(U)   The Bio-Electronics and Photonics program will demonstrate new capabilities in biologically derived optical and electronic media and devices. The thrust will explore highly promising organic and biological materials, such as Deoxyribonucleic Acid (DNA), proteins and novel nucleic acid-like materials that have the potential to fundamentally change the way that we develop and process electronics. The novel use of these materials has the potential to produce the biological analog of band gap and heterostructure engineering. This program will develop techniques for inclusion of such biological materials in a myriad of electrical devices ranging from diodes to batteries. The primary objective of this program is toward improved performance and lower costs. Examples of improved device performance would be reduced leakage current and faster switching times in field effect transistors, two areas that have shown promise in the recent breakthrough of the first DNA Schottky Diode. Other possible advantages are devices that are more compact, robust, environmentally friendly, require less power; and are amenable to flexible, just-in-time manufacturing; and has the potential to leverage the well established techniques such as combinatorical chemistry and high throughput nucleic acid sequencing. Results from this effort have the potential to: improve the performance of electronic devices, create new computational constructs, and define unique biotic-abiotic interfaces.

(U)   Program Accomplishments and Plans:
    FY 2007 Accomplishments:
    −   Developed process for room temperature fabrication of electronic materials with improved efficiency.
    −   Demonstrated 10x improvement in optical properties for high density storage with protein expression.
    −   Explored the integration of biological materials with several types of optical and electronic media and devices.
    −   Characterized the electrical properties of DNA Shottky Barrier Devices.
    FY 2008 Plans:
    −   Develop computational models for designing novel biological materials for electronic media and devices.
    −   Develop computational models of DNA Shottky Barrier Devices to model the electron interaction at the DNA/metal interface, as well as the movement of the band gap barrier height.
    −   Develop new materials for device fabrication taking the computational models into account.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, Project ELT-01

− Demonstrate electronic devices fabricated with novel biological materials. These devices will have improved performance (e.g. current leakage, switching times) over standard electrical devices.

	FY 2007	FY 2008	FY 2009
Chip-to-Chip Optical Interconnects	3.355	2.000	1.000

(U)   Continuing advances in integrated circuits technology are expected to push the clock rates of Complimentary Metal-Oxide Semiconductor (CMOS) chips into 10 gigahertz (GHz) range over the next five-to-seven years. At the same time, copper-based technologies for implementing large number of high-speed channels for routing these signals on a printed circuit board and back planes are expected to run into fundamental difficulties. This performance gap in the on-chip and between-chip interconnection technology will create data throughput bottlenecks affecting military-critical sensor signal processing systems. To address this pressing issue, this program developed optical technology for implementing chip-to chip interconnects at the board and back plane level.

(U)   Program Plans
FY 2007 Accomplishments:
− Developed high-linear density, low-loss optical data transport channels that can be routed to ~1 meter distance in a geometric form factor compatible with a printed circuit board.
− Demonstrated high-speed (faster then 10 billions of bits per second (GBps)), low-power (less then 50 mW) optical transmitters/receivers.
FY 2008 Plans:
− Integrate optical transmitters/receivers and optical data paths with electronic packaging.
FY 2009 Plans:
− Complete integration activities and manufacturing approaches.

	DATE
RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

	FY 2007	FY 2008	FY 2009
Photonic Analog Signal Processing Engines with Reconfigurability (PhASER)	0.000	9.000	7.891

(U)   The goal of the Photonic Analog Signal Processing Engines with Reconfigurability (PhASER) program is the creation of new Photonic Integrated Circuit (PIC) elements, and associated programmable filter array concepts that will enable high-throughput, low-power signal processors. The focus is on the development of novel "Unit Cells," which may be used as building blocks to synthesize arbitrarily complex filters within a PIC platform for ultra-high bandwidth signal processing applications.

(U)   Program Plans:
FY 2008 Plans:
 − Define and design a novel analog photonic "Unit Cell," which is nominally comprised of a sub-array of waveguide-connected programmable active elements. The Unit Cell should be externally linkable with integrated waveguides, which will allow it to function as a building block in programmable PIC arrays for generalized high-order finite impulse response/infinite impulse response (FIR/IIR) filters.
FY 2009 Plans:
 − Demonstrate an experimental Unit Cell concept.
 − Determine how the Unit Cell, when arrayed within a high-density PIC, will perform.
 − Develop a filter synthesis tool to demonstrate how Unit Cells will enable generalized high-order filters.
 − Determine how unit cells will be programmed and tested at the chip-level to ensure high yield.

	FY 2007	FY 2008	FY 2009
Linear Photonic RF Front End Technology (PHOR-FRONT)	7.266	4.594	6.385

(U)   The goal of the Linear Photonic RF Front End Technology (PHOR-FRONT) program is to develop photonic transmitter modules that can adapt their frequency response and dynamic range characteristics to mate with the full spectrum of narrow-band and broadband microwave

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	**DATE** February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

transmission applications covering the 2 megahertz (MHz) – 20 gigahertz range. These field programmable, real-time adaptive photonic interface modules will find application in high dynamic range communications, radar and Electronic Warfare antenna applications.

(U)   Program Plans:
    FY 2007 Accomplishments:
    −   Demonstrated photonic demodulation and optical down conversion; >56 decibels (dBs) spurious free dynamic range (SFDR) measured over a 333 MHz instantaneous bandwidth for an radio frequency (RF)-to-intermediate frequency (IF) link.
    −   Demonstrated phase demodulator with all-optical phase-locked loop with SFDR of more than 124 dB- hertz (Hz) 2/3 with 3 megampere of photocurrent.
    −   Demonstrated < 10 Hz Full Width Half-Maximum laser line-width with locked "slow light" fiber laser.
    −   Compounded doping of glass for laser outputs of more than 500 megawatts.
    FY 2008 Plans:
    −   Develop narrow line-width, 1,550 nanometer (nm) lasers with improved efficiency, relative intensity noise (RIN), and stability.
    −   Develop compact linear photonic receivers with improved sensitivity and dynamic range.
    FY 2009 Plans:
    −   Develop and enhance narrow line width, 1,550 nm lasers with world record efficiency, RIN, and stability in a compact package.
    −   Develop and enhance compact and packaged linear photonic receivers with world record sensitivity and dynamic range.

	FY 2007	FY 2008	FY 2009
Optical Arbitrary Waveform Generation (OAWG)	15.636	6.964	4.284

(U)   The ultimate vision for the Optical Arbitrary Waveform Generator (OAWG) program is to demonstrate a compact, robust, practical, stable octave-spanning optical oscillator, integrated with an encoder/decoder capable of addressing individual frequency components with an update rate equal to the mode-locked repetition rate. This would provide an unprecedented level of performance for optical systems, and enable numerous high-level applications including sub-diffraction-limited imaging and ultra-wide band optical communications.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

(U)   Program Plans:
FY 2007 Accomplishments:
- − Demonstrated 100 gigahertz (GHz) positive linear chirp with <5% least-squared deviation from mathematical ideal waveform.
- − Demonstrated production of single-cycle, 1.5 GHz square wave with fidelity of <5% least-squared deviation from mathematical ideal waveform.

FY 2008 Plans:
- − Develop 10 GHz octave-spanning carrier-envelope stabilized laser with integrated molecular frequency standard.
- − Design and build miniature 10 gigabyte/s multi-channel, parallel bit-error rate testbed for integrated system testing.

FY 2009 Plans:
- − Demonstrate 1,000 GHz positive linear chirp with <5% least-squared deviation from mathematical ideal waveform.
- − Demonstrate production of single-cycle, 3 GHz square wave with fidelity of <1% least-squared deviation from mathematical ideal waveform.

	FY 2007	FY 2008	FY 2009
Transparent Displays	0.000	0.000	3.000

(U)   The Transparent Displays program will develop technologies for the next generation of displays by leveraging the successes of previous programs in molecular electronics, as well as exploiting the optical plasmon phenomenology characteristics of nanoscale structures. Harnessing these tools will enable display systems that are transparent, low-power, light-weight, and high-speed. The new displays will replace existing displays in a host of applications, such as canopy-, windshield-, and window-integrated displays, and new light-weight avionics displays. Furthermore, the technology will enable innovative approaches to information sharing, such as integrated helmet display visors, bringing the digital battle space to the individual warfighter.

(U)   Program Plans:
FY 2009 Plans:
- − Develop new materials for thin, transparent, displays with daylight bright intensity using laser illumination.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	**DATE** February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

– Explore the use of new diffractive optics technology to provide lightweight optics with a comfortably viewable "virtual" image ahead of the viewer.

	FY 2007	FY 2008	FY 2009
Systems of Neuromorphic Adaptive Plastic Scalable Electronics (SyNAPSE)	0.000	0.000	3.000

(U)   The Systems of Neuromorphic Adaptive Plastic Scalable Electronics (SyNAPSE) program will develop a brain inspired electronic "chip" that mimics the function, capacity, size, and power consumption of a biological cortex. If successful, the program will provide the foundations for functional machines to supplement humans in many of the most demanding situations faced by warfighters today. In particular, the objective of the program is to process video images for information abstraction (e.g. annotation) and task initiation. The two main technical challenges to achieving this vision are developing an artificial electronic synapse and developing a neural algorithm-architecture that exploits these synapses.

(U)   Program Plans:
FY 2009 Plans:
– Develop hybrid CMOS and high-density synaptic crossbar arrays with density and function comparable to biological systems.
– Simulate large-scale neurally inspired systems using electronic device models.
– Develop standard testing protocols for assessing the performance of large neuromorphic electronic systems.

	FY 2007	FY 2008	FY 2009
Technology for Agile Coherent Optical Transmission & Signal Processing (TACOTA)	1.845	3.700	1.000

(U)   The goal of Technology for Agile Coherent Optical Transmission & Signal Processing (TACOTA) is to develop optoelectronic component technologies that enable increased physical layer security in optical transmission systems through the synergistic use of coherent optical technologies and high-speed electronics. Secure, high-capacity free-space communications is essential for the transformational communications architecture to be realized. Both digital and analog transmission will be considered.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	**DATE** February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, Project ELT-01

(U)   Program Plans:
FY 2007 Accomplishments:
−   Developed signal design and compensation methods for nonlinear transmission impairments that occur in optical fibers.
−   Developed indoor and outdoor testbeds to quantify advantages of mid-wavelength infrared versus short-wavelength infrared coherent optical communications.
−   Successfully modeled the Optical Parametric Oscillator Wavelength Translation Approach.
−   Demonstrated silica photonic crystal fiber based coherent wavelength translation between near-infrared and visible bands.
FY 2008 Plans:
−   Demonstrate multi-spectral coherent optical transmission and frequency (wavelength) translation with high conversion efficiency and narrow line-width.
−   FY 2009 Plans:
−   Complete final program demonstrations.

	FY 2007	FY 2008	FY 2009
Ultrabeam	2.626	2.188	3.419

(U)   The Ultrabeam program involved conversion of femtosecond duration ultraviolet laser light pulses to X-rays and the study of intense X-ray pulse propagation in various media.

(U)   Program Plans:
FY 2007 Accomplishments:
−   Achieved peak X-ray output pulses estimated to exceed the predicted critical power requirement for channel formation experiments.
FY 2008 Plans:
−   Demonstrated X-ray pulse spatial compression and observed preliminary indications of channel formation in a solid target.
FY 2009 Plans:
−   Create a Gamma Ray Laser between 100 KeV and 1 MeV.

	DATE
RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	February 2008

APPROPRIATION/BUDGET ACTIVITY	R-1 ITEM NOMENCLATURE
RDT&E, Defense-wide BA2 Applied Research	Electronics Technology PE 0602716E, Project ELT-01

	FY 2007	FY 2008	FY 2009
Photonic Bandwidth Compression for Instantaneous Wideband A/D Conversion*	0.000	3.235	4.445

*Formerly titled Ultra-Wideband A/D Conversion (UWB-ADC).

(U)   The objective of the Photonic Bandwidth Compression for Instantaneous Wideband A/D Conversion program is to develop revolutionary technologies to enable Analog to Digital Converters (ADCs) with high-resolution and large instantaneous bandwidth while maintaining power consumption that is commensurate with user community requirements. It is expected that such ADCs would have a dramatic impact on signals intelligence capabilities such as direct down conversion of ultra high frequency through X-band radio frequency (RF) signals. Furthermore, ADCs enabled by this program alleviate the current ADC bottleneck in high capacity digital RF communications links by enabling more spectrally efficient wideband waveforms. This program aims to develop a bandwidth-compressing photonic front end that provides a force multiplier for any available back-end electronic ADCs.

(U)   Program Plans:
    FY 2008 Plans:
    −   Demonstrate transient ADC with 6.5 estimated number of bits (ENOB) signal-to-noise ratio over a 10 gigahertz bandwidth.
    −   Develop a low-power ADC with high-dynamic range for an improved ENOB.
    FY 2009 Plans:
    −   Develop and enhance a low-power ADC with high-dynamic range for further improvement in the ENOB.

	FY 2007	FY 2008	FY 2009
Optical Antenna Based on Nanowires	0.000	2.000	1.000

(U)   In optics, nanotechnology research will develop the ability to create structures of the same scale as incident light wavelengths. These structures can interact with and affect the incident light. This program will create nano-meter scale structures, which will act as optical antenna arrays that can respond coherently to electromagnetic fields at optical wavelengths. Each array element would be a nanostructure, such as a nanotube or nanowire, and provide a way to measure directly the field magnitude and phase in both space and time. A system based on this

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, Project ELT-01

technology would potentially be smaller, lighter in weight, and able to move from the sub-optimal method of intensity-only measurements into the information-rich domain of complex imaging.

(U) Program Plans:
FY 2008 Plans:
− Study small element count two-dimensional array to identify performance and scaling relationships.
FY 2009 Plans:
− Characterize ability to measure the magnitude and phase of the incident light.

	FY 2007	FY 2008	FY 2009
3-D Microelectromagnetic RF Systems (3-D MERFS)	2.524	2.172	0.000

(U) The 3-D Microelectromagnetic RF systems (3-D MERFS) program will develop complete millimeter wave (MMW) active arrays on a single or a very small number of wafers. The program will exploit new technologies being developed commercially that allow Gallium Arsenide (GaAs) active components to be placed on Silicon wafers, and advances in Indium Phosphide and Silicon Germanium that may allow an entire MMW Electronically Scanned Array (ESA) to become very highly integrated on a sandwich of wafers. At lower frequencies, the large spacing between radiating elements precludes the efficient use of the wafer real estate for fabricating the entire ESA, but at Ka- and W- bands, the element spacing is small enough to allow an ESA to be made with active transmit/receive chips and control circuits on one layer, radiators on another, and a feed system on a third. This could potentially make them very cheap, compact, lightweight and reliable. This would enable the development of new MMW ESAs of a six inch diameter or less for seekers, communication arrays for point-to-point communications, sensors for smart munitions, robotics and small remotely piloted vehicles. This program will build upon technology developed under the Vertically Interconnected Sensor Array program.

(U) Program Plans:
FY 2007 Accomplishments:
− Demonstrated >99.9% yield on 1-centimeter transmission lines on individual wafers, a 300x increase in yield.
− Demonstrated 11-layer fabrication process, enabling transmission line cross-overs, low-loss transmission lines, and high-Q (energy ratio) resonators.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, Project ELT-01

− Demonstrated monolithically fabricated 16-beam (4 simultaneous) transmit/receive aperture.
− Established transition path for Sat-Com-on-the-Move application through Communications-Electronics Research, Development and Engineering Center (CERDEC) to PM/Warfighter Information Network Terrestrial (PM/Win-T).
− Established Phase IIB yield improvement plan to improve total yield for 1,000 element manifolds from 5% to the 50% needed for Sat-com-on-the-move application.
FY 2008 Plans:
− Demonstrate 50% total yield for 1,000 element manifolds.
− Demonstrate resistor and active element integration.
− Demonstrate ability to stack and tile MERFS substrates.

	FY 2007	FY 2008	FY 2009
Chip Scale Atomic Clock (CSAC)	5.000	4.519	4.471

(U)   The Chip Scale Atomic Clock (CSAC) will demonstrate a low-power chip scale atomic-resonance-based time-reference unit with stability better than one part per billion in one second. Application examples of this program will include the time reference unit used for Global Positioning System (GPS) signal locking.

(U)   Program Plans:
FY 2007 Accomplishments:
− Demonstrated feasibility and theoretical limits of miniaturization of cesium clock.
FY 2008 Plans:
− Demonstrate subcomponent fabrication including atomic chamber, excitation and detection function.
FY 2009 Plans:
− Demonstrate design and fabrication innovation for atomic-confinement cell and for gigahertz (GHz) resonators suitable for phase locking or direct coupling with atomic confinement cell.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	**DATE** February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

	FY 2007	FY 2008	FY 2009
Radio Isotope Micro-Power Sources (RIMS)	2.969	1.946	2.490

(U)   The Radio Isotope Micro-Power Sources (RIMS) effort will seek to develop the technologies and system concepts required safely to produce electrical power from radioisotope materials for portable and mobile applications, using materials that can provide passive power generation. There will also be research in compact radioisotope battery approaches that harness micro-electro-mechanical systems (MEMS) technology to safely and efficiently convert radioisotope energy to either electrical or mechanical power while avoiding lifetime-limiting damage to the power converter caused by highly energetic particles (e.g., such as often seen in previous semiconductor approaches to energy conversion). The goal is to provide electrical power to macro-scale systems such as munitions, unattended sensors, and weapon systems, radio frequency identification tags, and other applications requiring relatively low (up to tens of milliwatts) average power.

(U)   Program Plans:
FY 2007 Accomplishments:
–   Developed and demonstrated core technology for the direct capture of beta particles.
–   Demonstrated longevity for the chosen radioisotope-to-electrical power conversion technique.
FY 2008 Plans:
–   Demonstrate advances in power output and particle capture with high conversion efficiencies, while operating within safety considerations and limitations.
–   Demonstrate advanced dielectrics with high stability suitable for solid-state capture devices.
FY 2009 Plans:
–   Develop large-scale radioisotope generation cell based on beta particle capture.
–   Demonstrate actual, long-lasting power generation in a militarily useful form factor.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, Project ELT-01

	FY 2007	FY 2008	FY 2009
Micro Isotope Micro-Power Sources (MIPS)	8.033	2.201	0.000

(U)   The goal of the Micro Isotope Micro-Power Sources (MIPS) program is to demonstrate safe, affordable micro isotope power sources able to outperform conventional batteries in terms of energy and/or power density, and provide long lasting milliwatt-level power for an array of critical military applications, such as unattended sensors, perimeter defense, detection of weapons of mass destruction; and environmental protection.

(U)   Program Plans:
   FY 2007 Accomplishments:
   –   Fabricated boron carbide (BC) junctions with >10% conversion efficiency.
   –   Conducted survey of potential isotopes and determined isotopes most applicable to MIPS applications.
   FY 2008 Plans:
   –   Demonstrate radiation hardened BC junctions with >10% efficiency.
   –   Demonstrate thermophotovoltiac conversion system.
   –   Demonstrate thermo electric conversion system.

	FY 2007	FY 2008	FY 2009
Design Tools for 3-Dimensional Electronic Circuit Integration	4.589	7.474	1.000

(U)   The Design Tools for 3-Dimensional Electronic Circuit Integration program will develop a new generation of Computer Aided Design (CAD) tools to enable the design of integrated 3-dimensional (3-D) electronic circuits. The program will focus on methodologies to analyze and assess coupled electrical and thermal performance of electronic circuits and tools for the coupled optimization of parameters such as integration density, cross talk, interconnect latency and thermal management. The goals of this initiative are to develop a robust 3-D circuit technology through the development of advanced process capabilities and the design tools needed to fully exploit a true 3-D technology for producing high performance circuits. The deliverables from this program will have a significant impact on the design of mixed signal (digital/analog/radio

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

frequency) systems and Systems-on-a-Chip for high performance sensing, communications, and processing systems for future military requirements.

(U)   Program Plans:
   FY 2007 Accomplishments:
   – Demonstrated two-tier wafer-to-wafer bonding in both silicon-on-insulator and bulk complementary metal-oxide semiconductor (CMOS) technologies dense interlayer and thru-silicon via process.
   – Improved commercial off-the-shelf (COTS) chip-to-chip stacking process developed and tested in two-tier field-programmable gate array (FPGA) stacks twelve-tier chip-to-chip stack demonstrated without electrical interconnects.
   – Low temperature silicon, silicon germanium and germanium epitaxial growth processes developed to enable monolithic 3-D integration.
   – 3-D architecture studies were performed assessing the advantages of 3-D topologies for enhancing digital performance.
   – 3-D design kits, layout visualization and computer-aided design (CAD) tools were developed to enable 3-D design process.
   FY 2008 Plans:
   – Complete 3-D process technology development.
   – Choose several compelling applications to map into the 3-D technologies developed.
   – Begin fabrication of 3-D demo design chips.
   – Complete fabrication of 3-D demo design chips.
   FY 2009 Plans:
   – Assess performance gains due to 3-D topologies.

	FY 2007	FY 2008	FY 2009
Multiple Optical Non-Redundant Aperture Generalized Sensors (MONTAGE)	2.248	0.000	0.000

(U)   The Multiple Optical Non-Redundant Aperture Generalized Sensors (MONTAGE) program explored a revolutionary change in the design principles for imaging sensor systems; enabling radical transformation of the form, fit, and function of these systems for a wide variety of high-value DoD applications. Significant improvements in the performance, affordability, and deployability of imaging sensor systems were obtained

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	**DATE** February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

through rational co-design and joint optimization of the imaging optics, the photo sensor array and the post-processing algorithms. By reaching well beyond conventional designs, MONTAGE sensors will realize optimal distribution of information handling functions between analog optics and digital post-detection processing.

(U)   Program Plans:
FY 2007 Plans:
  −   Developed novel optical designs allowing depth reduction by 10x.
  −   Demonstrated ability to allocate highest spatial resolution to specified regions of interest in the image while maintaining medium resolution elsewhere.
  −   Demonstrated real-time performance of thin imaging systems in representative DoD applications with performance evaluated using application-specific metrics for image quality, sensor cost, power consumption, and mechanical properties.

	FY 2007	FY 2008	FY 2009
Polymorphous Computing Architecture (PCA)	5.802	0.000	0.000

(U)   The Polymorphous Computing Architectures (PCA) program developed a revolutionary approach to the implementation of embedded computing systems to support reactive multi-mission, multi-sensor, and in-flight retargetable missions. This revolutionary approach reduced the payload adaptation, optimization and verification processes from years to minutes. The program breaks the current development approach of hardware first and software last by moving beyond conventional silicon to flexible polymorphous computing systems. PCA architectures will adapt to efficiently perform a broad range of high-performance, challenging DoD processing functions utilizing a single architectural implementation.

(U)   Two promising PCA architectures, eXtended Tera-op Reliable Intelligently Adaptive Processing System (XTRIPS) and eXtended MOrphable Networked microARCHitecture (XMONARCH), have bridged the gap between the prototypes developed in the PCA program and the transition-ready solutions that can be adopted by DoD and intelligence agencies. This effort included performing product-level and prototype development of processor chips and software development environments planned for future deployment by DoD and intelligence end users.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, Project ELT-01

(U)   Program Plans:

FY 2007 Accomplishments:

− Successfully fabricated and delivered full implementation of the xMONARCH chip – first polymorphic computer – exceeding original goals.
− Successfully fabricated prototype TRIPS chip – first novel Explicit Data Graph Execution architecture computing chip - and supporting TRIPS compiler for implementing backend optimizations.
− Performed early small scale proof-of-concept testing, integration and evaluation of early polymorphic computing architecture prototypes – evaluation boards developed for both MONARCH and TRIPS devices.

	FY 2007	FY 2008	FY 2009
Vertically Interconnected Sensor Arrays (VISA)	5.200	0.000	0.000

(U)   The Vertically Interconnected Sensor Arrays (VISA) program developed and demonstrated vertically interconnected, focal plane array read-out technology capable of more than 20-bits of dynamic range – over an order of magnitude higher than current state-of-the-art – enabling significant advances in the functionality of infrared systems. Vertical interconnections between the detectors and the read-outs that avoid first going through row-column multiplexers will allow for high frame rates concurrent with high resolution images.

(U)   The VISA program expanded architectures for three-dimensional focal plane arrays, where multiple levels of signal processing were integrated into each pixel in the array, to include multiple processing layers, higher density vias (small openings in an insulating oxide layer that enable electrical connections, e.g., between layers) at the pixel, and coverage of a broad spectral band from the visible to the infrared. This increased on-chip processing power enabled new capabilities for smart sensors, such as high-speed imaging, on-chip threat discrimination, and anti-jamming. Defense applications include mid/long wavelength target acquisition systems for air and ground; smart missile seekers; anti-jamming; and imaging through high intensity sources. This program transitioned to PE 0603739E, Project MT-15.

(U)   Program Plans:

FY 2007 Accomplishments:

− Developed a wafer stacking process incorporating high-density vias and design novel circuits that enable high frame rates, counter-measure hardening and adaptive signal processing functions on a concept test chip.

	DATE
RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

- Demonstrated a high dynamic range Analog/Digital VISA technology based sensor designed with advanced high performance circuit architecture implemented in stacked semiconductor process with high-density interconnections.
- Determined the best bands for improving the detection of objects in varying degrees of fog.

	FY 2007	FY 2008	FY 2009
Novel Techologies for Optoelectronics Materials Manufacturing (NTOMM)	0.000	3.750	3.000

(U)   The goal of the Novel Technologies for Optoelectronics Materials Manufacturing (NTOMM) program is to develop and demonstrate new technologies for Group II-VI (e.g., Cadmium Selenide (CdSe)) and III-V (e.g., Gallium Nitride (GaN)) materials and device manufacturing, enabling imaging and emissive device fabrication at 1% to 10% current costs. This advance will dramatically expand the application space of such devices, by providing lower cost per large area infrared (IR) imaging systems, non-planar devices and systems, and thin film and flexible devices and systems. This program will demonstrate IR detectors and imagers, Light Emitting Diodes (LED), and solid-state lasers fabricated via new methods, and include a rapid demonstration of at least five times reduction in yielded device cost. The NTOMM program will leverage recent and ongoing developments in nano-material synthesis and assembly, which have demonstrated the potential for over 50% precursor stream usage in the fabrication of II-VI and III-V materials. An additional focus of the NTOMM program is the development of technologies to support the fabrication of low-cost high pixel density power efficient direct emission microdisplays. Current microdisplay systems use light modulation systems (Liquid Crystal Displays, Digital Micromirror Devices) and consequently only transmit a small fraction of the light from the illumination source thus limiting efficiency and use.

(U)   Program Plans:
FY 2008 Plans:
- Develop synthesis methods that improve quality and monodispersity (characterized by particles of uniform size in a dispersed space) of Indium nitride (InN) and Indium gallium nitride (InGaN) nanocrystals.
- Develop cost effective synthesis methods for Group II-VI and III-V materials.
- Utilize controlled arrays of InGaN to form high efficiency Light Emitting Diode (LED) structures and imaging sensors in infrared.
- Assemble layer-by-layer heterostructures (characterized by dissimilar materials with non-equal bandgaps) from ordered planar arrays of nanocrystals.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, Project ELT-01

− Develop and demonstrate techniques for layer doping of heterostructure materials.
− Evaluate and select approaches for the development of affordable emissive microdisplays.
FY 2009 Plans:
− Demonstrate initial device concepts.
− Select fabrication technologies with 5x cost reduction potential.
− Demonstrate fabrication technologies that support the fabrication of affordable emissive microdisplays.

	FY 2007	FY 2008	FY 2009
Structured ASIC Design (StASD)	0.000	3.500	5.500

(U)   Currently Application Specific Integrated Circuits (ASIC) have a 20-30x performance advantage over general-purpose programmable processors, this performance advantage is critical for high performance systems and platforms. Current ASIC design solutions are high in cost, require extensive time to design, apply to a single application, and need dedicated hardware; making them unattainable for most critical DoD systems. Also, when customizing ASICs for multiple applications, the overhead costs greatly increase resulting in reduced performance density, reduced clock speeds, and higher power. The development of a Structured ASIC Design (StASD) capability will provide the performance advantages of a customized ASIC but without the high overhead costs of programmable or fine-grain reprogrammable devices. The result will be highly novel, customizable ASICs that will dramatically enhance DoD application processing capabilities in terms of cost, time to design, and performance.

(U)   Program Plans:
FY 2008 Plans:
− Complete studies establishing the potential impact and underlying principles of structured ASIC approaches and perform the initial analysis of selected potential approaches.
FY 2009 Plans:
− Determine which common high performance functional elements provide the best option for high performance functionality and the appropriate level and capability of interconnects for optimal customization.
− Investigate and evaluate potential architectures and implementations for structured ASIC.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, Project ELT-01

	FY 2007	FY 2008	FY 2009
Cognitively Augumented Design for Quantum Technology (CAD-QT)	2.000	4.000	5.000

(U)   The Cognitively Augmented Design for Quantum Technology (CAD-QT) program has developed learning-based optimization tools and represents a stepping stone towards an intelligent search engine capable of guiding the designer through the complex trade spaces of quantum device design.

(U)   Program Plans:
FY 2007 Accomplishments:
-   Validated CAD-QT system by employing it to design optoelectronic modulator devices performing significantly beyond the current state-of-the-art.
-   Investigated the exploitation of new fields of nanophotonics and plasmonics in which metal nanostructures converted electromagnetic radiation into charge density waves.
FY2008 Plans:
-   Demonstrate the next generation CAD-QT tool to include thermoelectric coolers which employ superlattices to discriminate electrons and photons.
FY 2009 Plans:
-   Determine methods of controlling the ultimate CAD-QT product.
-   Apply diffusion graph data organization/dimensionality reduction to biological data.

	FY 2007	FY 2008	FY 2009
Non-Linear Math for Mixed Signal Microsystems	4.563	1.339	0.000

(U)   The principal goal of the Non-Linear Math for Mixed Signal Microsystems program is to demonstrate a significant linearity enhancement capability based upon a digital signal processing approach, implemented in a high performance, very large scale integration (VLSI) chip that will enable wideband high-dynamic range sensor systems to be developed in a cost effective manner.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	**DATE** February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

(U)   Program Plans:
FY 2007 Accomplishments:
− Developed broadly applicable methodologies for exploiting novel encoding strategies, closed loop adaptive equalization, integration of sensing and processing, and application-specific knowledge in order to provide revolutionary advances in information conversion.
− Explored novel architectures leveraging intelligent pre-processing based upon space, time, and mathematical transformations of analog measurements and employing cooperative integration of analog and digital processing to obtain required system level performance.
FY 2008 Plans:
− Work with new classes of quantization devices based on novel "error correcting" representations of numbers, such as beta encoders, phase encoders, geometric invariants.

	FY 2007	FY 2008	FY 2009
THz Transistors (TT)	0.000	0.000	3.000

(U)   The THz Transistors (TT) program will develop the technologies for terahertz (THz) transistors by following recently-established scaling laws for indium phosphide (InP) heterojunction bipolar transistors (HBTs). This program will focus on developing transistors larger than 1THz. In addition, the target integration level will be ~1000 transistors, sufficient for the circuit building blocks. Demonstration circuits will be >400 gigahertz (GHz) frequency dividers, >700 GHz power amplifiers, and a more complex mixed signal circuit at the end of the program. This program will address these super-scaled InP transistor challenges with innovative band gap engineering at the base and collector regions, aggressive reduction of the contact resistances and junction capacitances, reliable patterning processes for sub-100 nanometer emitter, and development of a multi-level dense interconnect process. Pushing into unchartered frequency domains, the testing, calibration, and modeling of THz transistors and circuits will also be addressed in this program.

(U)   Program Plans:
FY 2009 Plans:
− Scale the state-of-art transistors to record operating speed and develop associated device models.
− Develop an integration process and fabricate simple demonstration circuits.

	DATE
RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

− Develop a high yield fabrication process for complex demonstration circuits.

	FY 2007	FY 2008	FY 2009
Ultra Fast Lasers With Response > 100 GHz	0.000	0.000	2.000

(U)   The objective of the Ultra Fast Lasers with Response > 100 GHz program is to develop ultra-fast lasers with modulation response > 100 gigahertz (GHz) resonance frequency. The frequency response of directly modulated semiconductor lasers has been limited by the relaxation oscillation to ~ 40 GHz. This fundamental limit can be overcome by strong optical injection locking as demonstrated recently in vertical cavity surface-emitting lasers (VCSEL) and edge-emitting distributed feedback (DFB) lasers with enhanced resonance frequencies of 50 and 72 GHz, respectively. These are the highest ever reported for such lasers. Despite the impressive experimental demonstrations, the fundamental limit of such frequency enhancement was not well understood until very recently. A newly derived analytical expression for the maximum enhanced resonance frequency shows that it is proportional to the square root of the external injection ratio, and inversely proportional to the photon lifetime of the slave laser cavity. This new understanding makes it possible to engineer the resonance frequency and to design monolithically integrated laser structures with a tailored radio frequency (RF) response. This concept will lead to more efficient, higher power, millimeter-wave optoelectronic sources with the resonance frequency scaleable to ~ terahertz (THz).

(U)   Program Plans:
        FY 2009 Plans:
        − Investigate response of DFB and VCSEL.
        − Explore "all-optical" mode-locking by matching the resonance frequency with the cavity round-trip frequency of the slave laser.
        − Design monolithically integrated devices with the engineered RF response.

	DATE
RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

	FY 2007	FY 2008	FY 2009
DESTINY	0.000	0.000	3.000

(U)   The goal of Design-space Exploration and Synthesis Technology for Integrating Nontraditional Microsystems at Yield (DESTINY) program is to introduce a rational methodology for co-design of mixed signal systems with embedded fine-grain re-configurability and compensation. Beyond enabling the optimal application of compensation for high yield and adaptability in mixed signal function, such a design discipline would also lead to very new systems, which will dramatically change the accepted notions among customary component subsystems, buffer amplifiers, mixers, and digitizers. For instance, traditional hard tradeoffs between noise figure and linearity in front end amplifiers can be broken by deliberately designing nonlinearities, which ease the design of low noise figures without impairing system function through use of Non-Linear Equalizer (NLEQ) for overall improved system performance. The program will combine advanced ideas from robust optimization mixed signal architecture and design expertise from DoD and commercial companies, nonlinear signal processing expertise.

(U)   Program Plans:
FY 2009 Plans:
−   Establish methodologies to manage complexity in design trades through recent advances in fast, low-rank updates in physical models and distributed optimization.

	FY 2007	FY 2008	FY 2009
Ideal Channel Electronics (ICE)	0.000	0.000	2.400

(U)   The objective of the Ideal Channel Electronics (ICE) program will be to develop the ideal channel field effect transistor (FET), with a composite channel integrating highly mismatched semiconductors in order to achieve unprecedented performance levels. The ICE FETs will enable ultra-high-speed high-power amplifiers, which are critical for high-performance wideband transmitters. One example of ICE will be to integrate an ultra-high mobility channel with a high-breakdown sub-channel for an ultra-fast high-power FET that does not exist today. Successful integration of different semiconductors to form a FET channel will demand no or little degradation in charge distribution and transport properties, i.e. maintaining high mobility and charge concentrations in the channels as well as introducing minimal and tolerable defects. The approach will

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, Project ELT-01

be to develop methods for composite channel integration, such as wafer fusing the high mobility channel to the high breakdown channel or selective epitaxial regrowth. Significant technical challenges to be addressed include minimizing defects, which will affect the channel properties, alignment and bonding; methods to achieve mechanical integrity of dissimilar materials; and the achievement of high fabrication yields.

(U)   Program Plans:
FY 2009 Plans:
  −   Develop mechanical integrity of dissimilar materials.
  −   Develop high fabrication yields.

	FY 2007	FY 2008	FY 2009
Ultra-Low Power Subthreshold Electronics (UPSE)	0.000	0.000	3.000

(U)   The Ultra-Low Power Subthreshold Electronics (UPSE) program will achieve a >10x reduction in energy consumption for integrated circuits by developing technology that allows for circuit operation at the physical limits of power supply voltages. The objective of the UPSE program is to develop a circuit technology that will allow operation of devices in the subthreshold regime (≤ 0.3 V) in contrast to the typical super-threshold regime (≈ 1.0V). Particular emphasis is placed on the use of standard commercial complementary metal-oxide-semiconductor (CMOS) technology avoiding the need for specialized custom device fabrication. Application-specific parallelism will be leveraged for maintaining adequate performance in the sub-threshold regime while still consuming minimal power. A demonstration sensor or communication integrated circuit (IC) of significant military interest showing compelling low power performance and new mission capabilities will be built.

(U)   Program Plans:
FY 2009 Plans:
  −   Develop subthreshold standard cell library for application specific integrated circuit (ASIC) designs in a state-of-the-art commercial CMOS foundry process.
  −   Identify candidate IC designs of DoD interest that could demonstrate ultra-low power sub-threshold performance.

	DATE
RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

	FY 2007	FY 2008	FY 2009
Precision Opto-Mechanics - Mechanical Properties of Light	0.000	0.000	3.000

(U)   The Precision Opto-Mechanics - Mechanical Properties of Light program will develop new optomechanical devices that utilize enhanced optical gradient forces within resonant nano-optical cavities for all-optical actuation and sensing. Specific target applications will include optically controlled nano-mechanical resonators and optically tunable filters. One area of application is the use of optical force to drive the coupling of guided modes across a small gap between a waveguide and the coupled resonator. This will lead to optical tuning of nano-mechanical resonators with a resonance frequency exceeding 1 gigahertz (GHz). Radio frequency (RF) filters and reference oscillators based on on-chip resonators offer a solution to the increasing count of RF components needed in miniaturized wireless systems.

(U)   Program Plans:
FY 2009 Plans:
  − Demonstrate all-optical tuning of a nano-mechanical resonator with a resonance frequency greater than 1 GHz.
  − Demonstrate dynamic storage and release of optical pulses (10-100 per second) within the coupled double-layer resonator.
  − Determine the bandwidth and sensitivity limits of optically driven resonators.

	FY 2007	FY 2008	FY 2009
Raman Beam Combining and Cleanup	0.000	0.000	3.000

(U)   The objective of the Raman Beam Combining and Cleanup program is to develop a fundamentally new beam combining technology for delivering high brightness, diffraction limited and tunable output beams in the Mid-Wave infrared (MWIR). The approach does not require phase locking or wavelength locking of input lasers, yet there is no compromise in power or beam quality. Outputs from an array of free running MWIR lasers (such as quantum cascade laser) are added together to form a diffraction limited output with no loss of intensity or beam quality arising from their random relative phases. In the proposed approach, a multimode silicon Raman laser will provide the seed for a silicon power amplifier that exploits Raman amplification along with the Talbot effect in a multimode waveguide. While the resulting pump mode may have high aberration, the laser output will have a clean diffraction limited mode profile with high on-axis intensity. As a ubiquitous beam combiner that is agnostic with

<table>
<tr><td rowspan="2">RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)</td><td>DATE</td></tr>
<tr><td>February 2008</td></tr>
</table>

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, Project ELT-01

respect to input laser technology, this technology enables scalable high brightness diffraction limited output and has enormous potential as an efficient, compact, and robust source for infrared countermeasures and low noise MWIR amplification for chemical biological weapon detection.

(U)   Program Plans:
FY 2009 Plans:
- Convert low quality pump into a diffraction limited beam.
- Combine multiple pumps via self imaging in multimode waveguide.

	FY 2007	FY 2008	FY 2009
SWEEPER	0.000	0.000	4.000

(U)   The objective of the Short-range Wide-field-of-regard Extremely-agile Electronically-steered Photonic Emitter and Receiver (SWEEPER) program is to develop chip-scale dense waveguide modular technology to achieve true embedded phase array control for beams of ~10W average power, < 0.1 degree instaneous field of view (IFOV), > 45 degree total field of view (TFOV), and frame rates of > 100 Hertz in packages that are "chip-scale." Such performance will represent a three order of magnitude increase in speed, while also achieving a greater than two order of magnitude reduction in size. Additionally, the integrated phase control will provide the unprecedented ability to rapidly change the number of simultaneous beams, beam profile, and power-per-beam, thus opening up whole new directions in operational capability. Key technical challenges will center the ability to achieve the needed facet density (facet pitch should be on the order of a wavelength or two), control the relative phase across all facets to ~ 9-bits, and efficient coupling and distribution of coherent light to facets from a master laser oscillator with an integrated waveguide structure. Related projects and studies have pointed to the significant system-level pay-offs of the new proposed technology.

(U)   Program Plans:
FY 2009 Plans:
- Create a chip-scale optical beam forming and scanning technology.
- Combine architecture and technology to address integrated control of phased optical signals.

	DATE
RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

	FY 2007	FY 2008	FY 2009
Analog-to-Information (A-to-I)	0.000	0.000	3.000

(U)   The Analog-to-Information (A-to-I) program will develop and demonstrate the practical advantages of several specific suggestions for mechanization uncovered in the study phase, whose further development is likely to provide dramatic breakthroughs in digitization techniques and hardware. Success in this program will show the way to hardware and system advances enabling accurate extraction of useful information from broadband environments crowded with diverse signals and interference spread over a large dynamic range, as required to meet DoD's requirements for radio frequency (RF) applications of the present and the future. Additionally, by extracting signals of interest during the measurement phase, A-to-I based approaches reduce the bandwidth and resolution requirements of analog-to-digital converters, and simultaneously reduces the data glut that impacts downstream processing of digitized signals.

(U)   Program Plans:
FY 2009 Plans:
–   Systematically exploit practical hardware and software implementations of the most promising approaches from study phase: compressive sampling, variable projective unfolding, and nonlinear affine encoders.

	FY 2007	FY 2008	FY 2009
Frequency Domain Analog Optical Signal Processor	0.000	0.000	4.000

(U)   The objective of the Frequency Domain Analog Optical Signal Processor program is to develop an analog signal processor, which is capable of processing the equivalent of one teraflop per watt in the frequency domain. This program will require the development of large photonic integrated circuit-based filter arrays and associated photonic components which are many times more complex than the current state of the art.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, Project ELT-01

(U)   Program Plans:
FY 2009 Plans:
- Implement an analog vector-matrix-multiply operation by utilizing programmable, high-quality, micro-ring-resonator filters arranged in a matrix to multiply and add photonic signal inputs.
- Develop an integrated frequency domain analog optical signal processor to enable improved signal processing capabilities for improved radio frequency communication, laser radar, bio-sensing, and optical computing capabilities on platforms such as unmanned aerial vehicles.

	FY 2007	FY 2008	FY 2009
J-Band Advanced Digital Receiver (JADR)	0.000	0.000	2.400

(U)   Exploiting the pioneering architectural breakthroughs of the Digital Receiver program will create the next generation of analog-to-digital converters in low-power (4W) silicon germanium (SiGe) chip/complementary metal-oxide-semiconductor (CMOS) decoder chip integrated into a compact flip chip package. J-Band Advanced Digital Receiver (JADR) extends its impact into the J-band (10 gigahertz (GHz) to 20 GHz) by aggressive integration into scalable SiGe technology.

(U)   Program Plans:
FY 2009 Plans:
- Direct radio frequency sampling strategies for 1-20 GHz input range.
- Devise and optimize SiGe/CMOS Monolithic RF Noise Shaping Modulator.

	FY 2007	FY 2008	FY 2009
REceivers Power Optimized for Reconnaissance and Tagging (REPORT)	0.000	0.000	4.000

(U)   The goal of the REceivers Power Optimized for Reconnaissance and Tagging (REPORT) program is to demonstrate a 2.45 gigahertz (GHz) wake-up receiver, which will only consume less than 250 microwatts of power (~100X reduction) and will need < 10 Pico watt of the radio

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	**DATE** February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

frequency (RF) input power to wake up the circuit (> 10^6x reduction). Additionally, this receiver will contain all necessary functions, including low-noise RF amplification, demodulation, baseband processing, wake-up decision logic and power conversion functions. To achieve these challenging power goals and necessary functionalities, the program will focus on the following technical developments. First, short-gate-width enhancement-mode High Electronic Mobility Transistor technologies will be developed to achieve low-noise RF gain at extremely low DC power levels. In addition, multi-layer interconnect process will be developed to monolithically integrate high-Q (~100), very high resonant impedance load inductors, which are critical to provide RF gain for low-power amplifier stages. Furthermore, innovative complimentary metal-oxide-semiconductor circuit designs will be explored to smartly utilize and manage bias currents for reducing total power consumption while providing necessary logic and signal processing capabilities.

(U)   Program Plans:
FY 2009 Plans:
− Achieve low-noise RF gain at extremely low DC power levels.
− Integrate very high resonant impedence load inductors to provide necessary RF gain for low-power amplifier stages.

	FY 2007	FY 2008	FY 2009
Computational Imaging (CI)	0.000	0.000	3.000

(U)   The Computational Imaging (CI) program seeks to develop new imaging constructs that exploit the full information content (intensity, phase, and frequency) at the detection plan to perform real-time image processing in the analog domain. This imagery will be combined with advanced digital image processing algorithms to leverage the unique image plane information for more rapid image analysis and target identification.

(U)   Program Plans:
FY 2009 Plans:
− Develop image processing algorithms.
− Initiate the development of new imaging devices.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, Project ELT-01

	FY 2007	FY 2008	FY 2009
Non-contact EEG Technologies (NET)	0.000	0.000	3.000

(U)   The goal of the Non-contact EEG Technologies (NET) program is to develop a non-contact Electroencephalograph (EEG) system based on new electric field sensor designs. The sensors would have performance characteristics to measure the electric field due to brain activity (0.5-21 hertz (Hz) signal with 500 nV/Hz½ sensitivity) and be compact enough to mount on a light-weight cap or inside a warfighter's helmet. The signal from the individual sensors would then be collected and sent wirelessly to a unit mounted on the subject for further processing. The main challenges are to develop high sensitivity sensors in a small form factor, overcome one over frequency noise in sensing the electric fields and in multiplexing the sensor array to produce a high spatial resolution image of brain activity. In order to transition the EEG system to the brain monitoring community (both DoD and universities), the developed system's performance will be validated versus state-of-the-art wet electrode systems under a variety of operational situations.

(U)   Program Plans:
FY 2009 Plans:
  − Develop sensor technology to measure the electric field of brain activity.
  − Demonstrate single non-contact sensor for EEG.

	FY 2007	FY 2008	FY 2009
Ultra Low Loss Photonic Integrated Circuits and Processors	0.000	0.000	3.000

(U)   The Ultra Low Loss Photonic Integrated Circuits and Processors program will realize high time-bandwidth products in planar optical waveguide technologies, thereby enabling compact, low power, high dynamic range frequency processors for signals intelligence (SIGINT) and imagery intelligence (IMINT).

	DATE
RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	February 2008

APPROPRIATION/BUDGET ACTIVITY	**R-1 ITEM NOMENCLATURE**
RDT&E, Defense-wide BA2 Applied Research	Electronics Technology PE 0602716E, Project ELT-01

(U)   Program Plans:

FY 2009 Plans:

   − Develop an on-chip, ultra low-loss waveguide technology.

   − Develop and enhance an on-chip, ultra low-loss waveguide technology to meet desired "fiber-like" performance.

	FY 2007	FY 2008	FY 2009
Processing Algorithms with Co-design of Electronics (PACE)	0.000	0.000	3.000

(U)   The Processing Algorithms with Co-design of Electronics (PACE) program enables the co-design of the next generation of embedded signal processing algorithms and architectures capable of processing large sparse matrix data structures associated with graph structured signal processing algorithms. Graph algorithms are the key to post-detection signal processing, helping to "connect the dots" in a huge variety of emerging challenges ranging from social network analysis, change detection in massive data transactions, and forensic and predictive analyses of activities from video data over wide areas and extended times. The goal of the PACE program is to provide the DoD with an architecture and algorithm co-design capability for what is likely to be the next big thing in DoD embedded signal processing: Graph-structured signal processing. Solutions available today that might meet these mission requirements are limited by prohibitively long and costly manual design times. The PACE program will provide signal processing capabilities not possible today while achieving dramatically reduced design time and cost.

(U)   Program Plans:

FY 2009 Plans:

   − Recast algorithms into sparse arrays.

   − Co-design mapping to novel high performance computing architectures.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	**DATE** February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

	FY 2007	FY 2008	FY 2009
Visible InGan Injection Lasers (VIGIL)	0.000	2.000	5.382

(U)   The objective of the Visible InGan Injection Lasers (VIGIL) program is to demonstrate injection lasers emitting in green, at l=500 nanometers (nm). Specific program goal is to demonstrate green injection lasers operating continuous wave at room temperature with the power output up to 1 watt (W), wallplug efficiency of 30%, and stable output during a time period longer than 1,000 hours. These lasers will be fabricated with a yield of 20%. VIGIL lasers will enable applications requiring a close match between the light source and the peak response wavelength of the human eye. Another class of applications will take advantage of the minimum absorption of sea water in the blue-green spectral region. Diverse other applications include miniaturized displays and pumps for generation of high-frequency mode-locked combs.

(U)   Program Plans:
FY 2008 Plans:
−   Scale the output power of the laser to at least 100 milliwatts (mW).
−   Achieve wallplug efficiency of 20%, stable operation of 500 hrs.
−   Demonstrate wafer yield of at least 10%.
FY 2009 Plans:
−   Demonstrate room temperature 500 nanometer lasers and validate the technical approach for device demonstrations.
−   Scale the output power of the laser to at least 100 mW, achieve wallplug efficiency of 20%, stable operation of 500 hours, and demonstrate wafer yield of a least 10%.

	FY 2007	FY 2008	FY 2009
Quantum Sensors	0.000	0.000	7.000

(U)   The Quantum Sensors program is developing approaches to exploit non-classical effects called entanglement to improve the resolution and range of military sensors. Quantum sensors will retain the generally better propagation characteristics of long wavelength light while achieving the better spatial resolution of short wavelength radiation. Conventional classical sensors rely on light with shorter wavelengths, like blue light, to

	DATE
RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

produce sharp images. As wavelengths increase, for example from blue to infrared, the classical resolution decreases. Quantum sensors will be able to retain high resolution as the wavelength increases using a non-classical effect called entanglement. Two broad classes of sensor are under consideration. Type I quantum sensors propagate entangled photons to a target and back to a detector, where quantum effects may enhance resolution. Type II quantum sensors propagate classical radiation to the target, and entangled photons are used within the detector to improve resolution. A third class of approach, based on ghost imaging, is also being explored. During the theoretical proof stage in FY 2007 to 2008 this program is funded under PE 0601101E, Project MS-01.

(U)   Program Plans:
FY 2009 Plans:
   −   Commence component technology development.
   −   Begin Quantum Sensor systems analysis to quantify achievable system performance and component technology requirements.

	FY 2007	FY 2008	FY 2009
Parametric Optical Processes and Systems (POPS)	0.000	1.000	2.142

(U)   The Parametric Optical Processes and Systems (POPS) program aims to direct terabits per second (Tb/s) optical switching to move ultra-short optical bits in time and wavelength to accomplish wavelength grooming. This program will develop disruptive manufacturing processes to reduce the cost and delivery time for future DoD systems.

(U)   Program Plans:
FY 2008 Plans:
   −   Develop basic building block components - multiple-pump amplifiers.
FY 2009 Plans:
   −   Initiate quantitative system demonstrations in wavelength grooming.
   −   Develop technology in highly nonlinear dispersion flattened fiber.

			DATE
RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)			February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

	FY 2007	FY 2008	FY 2009
National Secure Foundry Initiative	2.000	0.000	0.000

(U)   The Secure Advanced Fabrication Facility for Electronics (SAFFE) developed nanoelectronics innovations in support of homeland security and national defense applications with target products ranging from power electronics systems, advanced superconductors, integrated "nanochip" solutions for lithography, 3-Dimensional integration, device modeling and simulation, and metrology applications. Scaling down of semiconductor device feature sizes has led to advanced electronic components and new capabilities for signal and data processing.

(U)   Program Plans:
        FY 2007 Accomplishments:
        −   Pursued research concepts for shrinking semiconductor devices to the nanoscale and explored applications to integrated microsystems.

	FY 2007	FY 2008	FY 2009
Characterization, Reliability & Applications for 3-D Microdevices	2.600	0.000	0.000

(U)   The Characterization, Reliability & Applications for 3-D Microdevices explored innovative processes to improve the fabrication of 3-Dimensional (3-D) Microdevices.

(U)   Program Plans:
        FY 2007 Accomplishments:
        −   Developed innovative processing instrumentation for the fabrication of 3-D Microdevices.

		DATE
RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)		February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

	FY 2007	FY 2008	FY 2009
3-D Technology for Advance Sensor Systems	2.200	2.400	0.000

(U)   The 3-D Technology for Advance Sensor Systems effort will exploit 3-Dimensional (3-D) technology for applications in Advance Sensor Systems.

(U)   Program Plans:
FY 2007 Accomplishments:
−   Explored 3-D technology innovation for application to Advance Sensor Systems.
FY 2008 Plans:
−   Apply 3-D technology to device implementation.

(U) Program Change Summary: *(In Millions)*	**FY 2007**	**FY 2008**	**FY 2009**
Previous President's Budget	239.370	213.529	219.844
Current Budget	215.742	196.707	211.457
Total Adjustments	-23.628	-16.822	-8.387
Congressional program reductions	-7.500	-19.222	
Congressional increases	0.000	2.400	
Reprogrammings	-10.000		

	DATE
RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	February 2008

APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	**R-1 ITEM NOMENCLATURE** Electronics Technology PE 0602716E, Project ELT-01

SBIR/STTR transfer   -6.128

(U) **Change Summary Explanation:**

FY 2007   Decrease reflects the Section 8043 Recission, the DoDEA/DSS reprogramming, and the SBIR/STTR transfer.

FY 2008   Decrease reflects a PE execution adjustment and reductions for Section 8097 Contractor Efficiencies and Section 8104 Economic Assumptions; offset by a congressional add for 3-D Technology for Advanced Sensor Systems.

FY 2009   Decrease reflects minor rephasing of electronics programs.

(U) **Other Program Funding Summary Cost:**

- Not Applicable.