RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)							DATE February 2007	
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research			R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E					
COST (In Millions)	FY 2006	FY 2007	FY 2008	FY 2009	FY 2010	FY 2011	FY 2012	FY 2013
Total Program Element (PE) Cost	220.011	239.370	213.529	219.844	232.025	249.025	250.425	260.425
Electronics Technology ELT-01	220.011	239.370	213.529	219.844	232.025	249.025	250.425	260.425

(U) Mission Description:

(U) This program element is budgeted in the Applied Research budget activity because its objective is to develop electronics that make a wide range of military applications possible.

(U) Advances in microelectronic device technologies, including digital, analog, photonic and MicroElectroMechanical Systems (MEMS) devices, continue to have significant impact in support of defense technologies for improved weapons effectiveness, improved intelligence capabilities and enhanced information superiority. The Electronics Technology program element supports the continued advancement of these technologies through the development of performance driven advanced capabilities, exceeding that available through commercial sources, in electronic, optoelectronic and MEMS devices, semiconductor device design and fabrication techniques, and new materials and material structures for device applications. A particular focus for this work is the exploitation of chip-scale heterogeneous integration technologies that permit the optimization of device and integrated module performance.

(U) The phenomenal progress in current electronics and computer chips will face the fundamental limits of silicon technology in the early 21st century, a barrier that must be overcome in order for progress to continue. Another thrust of the program element will explore alternatives to silicon-based electronics in the areas of new electronic devices, new architectures to use them, new software to program the systems, and new methods to fabricate the chips. Approaches include nanotechnology, nanoelectronics, molecular electronics, spin-based electronics, quantum-computing, new circuit architectures optimizing these new devices, and new computer and electronic systems architectures. Projects will investigate the feasibility, design, and development of powerful information technology devices and systems using approaches to electronic device designs that extend beyond traditional Complementary Metal Oxide Semiconductor (CMOS) scaling, including non silicon-based materials technologies, to achieve low cost, reliable, fast and secure computing, communication, and storage systems. This investigation is aimed at developing new capabilities from promising directions in the design of information processing components using both inorganic and organic substrates, designs of components and systems leveraging quantum effects and chaos, and innovative approaches to computing designs

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

incorporating these components for such applications as low cost seamless pervasive computing, ultra-fast computing, and sensing and actuation devices. This project has five major thrusts:

- Electronics: The manipulation of electrons in digital, analog, and mixed signal circuits for sensing, processing, and communications. This thrust includes such programs as Advanced Digital Receiver, Advanced Microsystems Technology Program, Applications of Molecular Electronics (MoleApps), Clockless Logic; Energy Starved Electronics (ESE), High Frequency Wide Band Gap Semiconductor Electronics Technology, High Power Wide Band Gap Semiconductor Electronics Technology, HyperX, Metaphoric Computing, Nanowire Electronics and Optoelectronics, Quantum Information Science (QIS), Robust Integrated Power Electronics (RIPE), Submillimeter Wave Imaging FPA Technology (SWIFT), Technology Efficient Agile Mixed Signal Microsystem (TEAM),Technology for Frequency Agile Digitally Synthesized Transmitters (TFAST), Feedback-Linearized Microwave Amplifiers, Terahertz Imaging Focal-Plane Technology (TIFT), Trusted, Uncompromised Semiconductor Technology (TrUST), Co-integration of Carbon-Based rf Electronics with Silicon Technology (CrEST), Compound Semiconductor Materials On Silicon (COSMOS), Steep-subthreshold-slope Transistors for Electronics with Extremely-low Power, and Semiconductor-Tuned HTS Filters for Ultra-Sensitive RF Receivers (SURF).

- Photonics: The generation, detection, and modulation of photons for imaging, communications, and sensing. This thrust encompasses the following programs: Adaptive Focal Plane Arrays (AFPA), Advanced Precision Optical Oscillator (APROPOS), Analog Optical Signal Processing (AOSP), Bio-Electronics and Photonics, Chip-to-Chip Optical Interconnects, Photonic Analog Signal Processing Engines with Reconfigurability (PhASER), Linear Photonic RF Front End Technology (PHOR-FRONT), Optical Arbitrary Waveform Generation (OAWG), Technology for Agile Coherent Optical Transmission & Signal Processing (TACOTA), Solid State Imager/Extended Range Materials/Long Wave Length High Gain Optical Sensors, Ultrabeam, Bandwidth Compression for Power Efficient Ultra-WideBand Analog-to-Digital Conversion (UWB-ADC), Novel Technologies for Optoelectronics Materials Manufacturing (NTOMM), and Optical Antenna Based on Nanowires.

- MicroElectroMechancial Systems (MEMS): Exploitation of the processing tools and materials from semiconductor technology to build electro-mechanical structures at the micro- and nano-scale. The MEMS thrust encompasses: 3-D Microelectromagentic RF Systems (3-D MERFS), Chip Scale Atomic Clock, Radioisotope Micropower Sources (RIMS), Micro Isotope Micro-Power Sources (MIPS), and Surface Enhanced Raman Scattering (SERS) - Science and Technology.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

- Architectures: Exploitation of new arrangements of materials, devices, and circuits to increase performance or reduce power. Programs under this thrust include: Design Tools for 3-Dimensional Electronic Circuit Integration, Multiple Optical Non-Redundant Aperture Generalized Sensors (MONTAGE), Polymorphous Computing Architecture (PCA), Vertically Interconnected Sensor Arrays (VISA), Lidar on a Chip, and Structured ASIC Design (StASD).

- Algorithms: Exploitation of insights into mathematical constructs for data representation, process control, and discrimination routines by leveraging knowledge of Microsystem hardware operation. Programs under this thrust include: Cognitively Augmented Design for Quantum Technology (CAD-QT), Direct Analog To Target ID - Non-Linear Math for Mixed Signal Microsystems, and Reliable Efficient Scalable Computing with Unreliable Elements (RESCUE).

- Other Electronic Technology Research: National Secure Foundry Initiative; Semiconductor Nanoelectronics Research; Characterization, Reliability and Applications for 3-D Microdevices, and 3D Technology for Advance Sensor Systems.

(U) Program Accomplishments/Planned Programs:

	FY 2006	FY 2007	FY 2008	FY 2009
Advanced Digital Receiver	2.200	3.000	4.000	6.000

(U) The Advanced Digital Receiver program will leverage and improve Analog to Digital Converter (ADC) technology to develop Digital Receivers with greatly enhanced performance. Goals include reducing size, weight and power by an order of magnitude, enhancing programmability, flexibility and performance, reducing life cycle cost, and developing ADCs with 16 effective bits, 100 MHz instantaneous bandwidth and >100 dB spurious free dynamic range (SFDR).

(U) Program Plans:
- Demonstrate 1st Pass Sigma-delta Modulator in test fixture.
- Demonstrate 2nd Pass Sigma-delta Modulator in test fixture with ADC-Digital-to-Analog Converter (DAC) Iteration 1.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

- Demonstrate Real-time Digital Receiver Operation by Benchtop Integration of Best Sigma-delta Test Fixture and Wideband Agile Receiver Decoder Test Fixture.
- Demonstrate 3rd Pass Sigma-delta Modulator in test fixture with ADC-DAC Iteration 2.
- Demonstrate Real-time Digital Receiver Module Prototype (provide 5 modules).
- Direct RF sampling strategies for 1-20 GHz input range.
- Correct nonlinear errors of full operational bands.
- Devise and Optimize Silicon Germanium (SiGe)/Complementary Metal-Oxide Semiconductor (CMOS) Monolithic RF Noise Shaping Modulator.

	FY 2006	FY 2007	FY 2008	FY 2009
Advanced Microsystems Technology Program	5.000	5.000	0.000	0.000

(U) This program will explore a range of advanced microsystem concepts well beyond existing current technologies. The program will focus on technologies that exploit three-dimensional structures, new materials for Gieger mode detectors, advance patterning, and extreme scaling in silicon devices. Insights derived in these areas will be exploited in future program initiatives.

(U) Program Plans:

- Establish and exercise multi-project wafer runs for 3D integrated circuits.
- Demonstrate bonding and functionality of Silicon-On-Insulator circuits to Indium Phosphide detectors.
- Extend maskless multiple exposure system to 2x smaller features.
- Demonstrate photoresist capable of multiple in-situ exposure with enhanced resolution.
- Demonstrate sub-35 nm half-pitch interometric liquid exposure capability.
- Prepare report analyzing prospects for beyond roadmap technologies.
- Deliver data on ultra-low voltage operation of Silicon CMOS for DoD applications.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

	FY 2006	FY 2007	FY 2008	FY 2009
Applications of Molecular Electronics (MoleApps)	8.710	6.410	10.110	10.345

(U) The goal of the MoleApps program is to extend the capabilities being developed in the current Moletronics program to demonstrate the computational processing capabilities of molecular electronics in a system that integrates memory with control logic and data paths. A demonstration processor will be designed and built that can interpret a simple high-level language. This approach will allow the use of simpler processor designs to demonstrate the advantages of nano-scale molecular electronics that do not have the conventional circuitry overhead associated with modern pipeline chip designs.

(U) Program Plans:

- Construct combinatorial logic functions assembled from molecular-scale components.
- Use small-scale integration (SSI) to build combinatorial logic functions using molecular-scale components.
- Construct a sequential logic/finite-state machine assembled from molecular-scale components.
- Add registers or latches in communication with combinatorial logic arithmetic functions.
- Use medium-scale integration (MSI) to construct sequential logic/finite-state machine assembled from molecular-scale components.
- Demonstrate molecular electronics sensor array with 50 sensors per square micron capable of detecting 7 agents in 10 seconds with probability of detection > 0.99 and false positive $<10^{-5}$.
- Develop new mathematical theories to allow the construction of new circuit devices that are more efficient, economical, user-friendly, and which meet the physical constraints and computational needs.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

	FY 2006	FY 2007	FY 2008	FY 2009
Clockless Logic	3.700	1.500	0.000	0.000

(U) The goal of the Clockless Logic program is to develop techniques to reduce the amount of design resources required in chip design and significantly reduce the power and noise to provide improved system operation. Clockless methods will provide more efficient designs especially for military systems with demanding space, weight, power, and noise constraints.

(U) Program Plans:
- Developed method for design of complex chips using clockless logic.
- Enhanced tools and methods for design of clockless logic circuits and systems.
- Identified and designed complex chips with significant potential for improved system performance and reduced design times.
- Applied clockless design methods to programmable logic devices to provide significant potential for improved system performance and reduced design times.
- Demonstrate performance enhancements of complex chip enabled by clockless logic in radar or similar testbed.

	FY 2006	FY 2007	FY 2008	FY 2009
Energy Starved Electronics (ESE)	2.450	3.000	0.000	0.000

(U) The Energy Starved Electronics (ESE) program seeks to develop ultra low power integrated circuit devices and circuit design methods for military electronics that must operate where power is severely limited. The objective of the program is to mature both device technology and design techniques to allow operation of devices in the sub threshold (very low voltage) regime beyond where the circuit devices normally operate. The ability to operate an ultra-low power circuit while still maintaining modest performance will enable the successful implementation of many long lived operational systems such as remote sensor networks as well as small unit communications and other wireless applications. The goal of the program will be a 100X improvement in energy per operation over conventional designs operated at low voltage.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

(U) Program Plans:
- Develop a robust design methodology and sub-threshold standard cell library.
- Implement a feedback control scheme to achieve operation at the minimum energy dissipation point.
- Demonstrate ultra-dynamic voltage scaling methodology that allows performance and energy to be traded-off over several orders of magnitude.
- Establish fundamental limits of energy dissipation of digital circuits taking into account process variations and device impairments (e.g., leakage).

	FY 2006	FY 2007	FY 2008	FY 2009
High Frequency Wide Band Gap Semiconductor Electronics Technology	29.289	30.711	30.150	31.020

(U) The High Frequency Wide Band Gap Semiconductor Electronics Technology program is developing high performance, cost effective high power electronic devices that exploit the unique properties of wide band gap semiconductors. Specifically, this program will develop low defect epitaxial films, high yield fabrication processes, and device structures for integrated electronic devices for emitting and detecting high power radio frequency/microwave radiation, and high power delivery and control.

(U) Program Plans:
- Develop bulk and surface process technologies for reducing or mitigating crystallographic defects in wide band gap materials.
- Develop semi-insulating substrates for high frequency devices.
- Design high power enclosures for microwave electronic assemblies.
- Demonstrate large periphery high power devices suitable for microwave and mm-wave operation.
- Demonstrate process reproducibility and minimization of yield limiting factors.
- Establish device characterization for very high power solid-state amplifiers.
- Demonstrate 100 mm Silicon Carbide (SiC) and wide band gap alternate substrates with less than 80 micropipe/cm^2 and resistivity 10^6 ohms-cm.
- Demonstrate epitaxial processes that yield + 3 percent uniformity over 75 mm wide bandgap substrates.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

- Initiate thermal management study to determine best packaging approach for high power, high frequency microwave and millimeter wave transistors.
- Demonstrate 100 mm SiC and wide band gap alternate substrates with less than 40 micropipe/cm^2 and resistivity 10^7 ohms-cm.
- Demonstrate epitaxial processes that yield + 1 percent uniformity over 100 mm wide bandgap substrates.
- Identify fabrication processes for robust microwave and mm-wave devices.
- Identify thermal management concepts to sustain more than 1 KW/cm2 power density in high power devices.
- Optimize wide band gap semiconductor materials to achieve 100 mm substrates with less than 10 micropipe/cm^2 and resistivity greater than 10^7 ohms-cm at room temperature.
- Demonstrate fabrication processes for robust microwave and mm-wave devices with RF yields greater than 70 percent.
- Demonstrate thermal management concepts to sustain more than 1KW/cm^2 power density in high power device.

	FY 2006	FY 2007	FY 2008	FY 2009
High Power Wide Band Gap Semiconductor Electronics Technology	6.705	5.500	0.000	0.000

(U) An initiative in High Power Wide Band Gap Semiconductor Electronics Technology will develop components and electronic integration technologies for high power, high frequency microsystem applications based on wide band gap semiconductors.

(U) Program Plans:

- Developed low defect conducting Silicon Carbide (SiC) substrate consistent with yielding 1 cm^2 devices.
- Developed lightly doped, thick (more than 100 micron) SiC epitaxy with low defects to enable 10 kV class power devices.
- Developed low on-state resistance SiC diodes capable of blocking 10 kV.
- Demonstrated SiC wafer and thick epitaxy with less than 1.5 catastrophic defects per cm^2 consistent with 10 kV reverse blocking.
- Initiated work on Megawatt class SiC power device able to switch at more then 100 kHz.
- Initiated work on packaging of high power density, high temperature SiC power electronics.
- Demonstrate megawatt Class SiC power devices.
- Demonstrate high power density packaging for greater than 10 kV operations.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

– Develop integrated power control logic compatible with high temperature and power SiC power devices.

	FY 2006	FY 2007	FY 2008	FY 2009
HyperX	4.150	0.000	0.000	0.000

(U) Many Department of Defense (DoD) systems require processing and analysis of vast amounts of high-dimensional data in the field. The HyperX program provided the capability for high performance signal processing at significantly lower power in a reconfigurable architecture. The focus of the program was to provide the military with a reconfigurable integrated circuit technology that can achieve high performance application-specific real-time signal processing at low enough power to be suitable for embedded applications. In these cases, where severe constraints on power preclude the use of general purpose processing solutions, HyperX chips will provide more than an order of magnitude (10x) increase in both power and throughput performance over the current state-of-the-art reconfigurable Field Programmable Gate Array (FPGA) and general programmable processors.

(U) Program Plans:
- Demonstrated a novel, reconfigurable integrated circuit (IC) with significant improvement over current programmable and reconfigurable IC technology.
- Verified performance of HyperX IC fabric (operate at $\geq$ 500MHz and consume $\leq$ 250milliwatts).
- Developed Integrated Hardware/Software Design Environment Software.

	FY 2006	FY 2007	FY 2008	FY 2009
Metaphoric Computing	0.000	4.000	4.000	8.000

(U) Metaphoric computing is a dramatically different approach to computation than the predominant paradigm using digital representation and Complementary Metal-Oxide Semiconductor (CMOS) digital circuits consisting of logic gates. The conventional digital computing systems work by employing binary data representation and mapping the physics of CMOS transistors on the lowest level computation, namely the logic gate.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

Metaphoric computing exploits the physics of electronic and photonic systems to enable implementation of complex signal processing algorithms in real time on power-limited platforms. Similarly, modeling and simulations of nonlinear dynamical systems will be accelerated by many orders of magnitude by employing a physics-based approach to computation entailed in metaphoric computing initiative.

(U) Program Plans:
- Design photonic systems to display sophisticated dynamic behavior that is described by nonlinear partial differential equations.
- Transform equations to another set of equations that describe the spread of disease or turbulent fluid flow around a complex structure.
- Generate and manipulate asynchronous pulse train that is used to represent incoming signals over a wide dynamic range.
- Implement signal processing operation of Independent Component Analysis that is useful in blind signal separation problems.

	FY 2006	FY 2007	FY 2008	FY 2009
Nanowire Electronics and Optoelectronics	0.000	3.000	3.000	8.000

(U) The Nanowire Electronics and Optoelectronics program will synthesize, characterize, and apply new nanowire technologies for electronic, optoelectronic, and sensor applications, which will enable new types of high-performance, heterogeneous micro- and nanosystems. Additional new types of optoelectronic devices, interconnections, and nanodisplays are also envisioned. Nanowire cell probes capable of reporting intracellular transport processes may open a new type of *in vivo* cellular biosensing for the early detection of BW agent exposure. The program goal is to extend successful nanowire materials synthesis concepts on Silicon substrates into new micro- and nanosystems applications.

(U) Program Plans:
- Achieve controlled materials synthesis, patterning, and control of interface properties.
- Use low-temperature vapor-liquid-solid (VLS) growth of Gallium Arsenide on a lattice-mismatched Silicon substrate.
- Use nanodot nucleation surfaces to initiate vertical nanowire growth.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

	FY 2006	FY 2007	FY 2008	FY 2009
Quantum Information Science (QIS)	22.730	16.040	9.000	7.022

(U) The Quantum Information Science (QIS) program, formerly called the Quantum Entanglement Science and Technology (QuEST) program, will explore all facets of the research necessary to create new technologies based on quantum information science. Research in this area has the ultimate goal of demonstrating the potentially significant advantages of quantum mechanical effects in communication and computing. Expected applications include: new improved forms of highly secure communication; faster algorithms for optimization in logistics and wargaming; highly precise measurements of time and position on the earth and in space; and new image and signal processing methods for target tracking. Technical challenges include: loss of information due to quantum decoherence; limited communication distance due to signal attenuation; limited selection of algorithms and protocols; and larger numbers of bits. Error correction codes, fault tolerant schemes, and longer decoherence times will address the loss of information. Signal attenuation will be overcome by exploiting quantum repeaters. New algorithm techniques and complexity analysis will increase the selection of algorithms, as will a focus on signal processing. The QIS program is a broad-based effort that will continue to explore the fundamental open questions, the discovery of novel algorithms, and the theoretical and experimental limitations of quantum processing as well as the construction of efficient implementations.

(U) Program Plans:

- Refine quantum architecture and design solutions for problems such as graph isomorphism, imaging, and signal processing.
- Investigate alternative protocols for secure quantum communication, quantum complexity, and control.
- Integrate improved single and entangled photon sources and detectors into existing quantum communication networks.
- Investigate alternative designs, architectures and devices for quantum communication and demonstrate high-rate (1Gbit/sec) quantum-secure communication over a single link; transition quantum-secure communication to existing DoD mobile testbed.
- Investigate unresolved fundamental issues related to quantum information science.
- Employ qubit architectures to demonstrate an application of interest to the DoD (e.g., quantum repeater, secure metropolitan-area network).
- Demonstrate interoperation between multiple qubit types to interconnect quantum communications links.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

	FY 2006	FY 2007	FY 2008	FY 2009
Robust Integrated Power Electronics (RIPE)	5.580	8.753	4.808	0.000

(U) The RIPE program will develop new semiconductor materials, devices, and circuits that enable highly compact, highly efficient electronic power converter modules. These new modules will be capable of providing up to 50kW of power per module at a power density of 500W/cubic inch. Based on fundamental material properties, the new power modules will be capable of operating in harsh environments. These new power converters will reduce the launch weight of space-based platforms by hundreds of pounds and will enable new modes of operation where the power conversion is done at the point of load and provides high quality power to payloads. Application of RIPE on Naval surface ships would result in a significant reduction of power supply weight; allowing for additional electronic components and/or weapons.

(U) Program Plans:
- Identified key technical challenges and quantified impact on potential platforms.
- Perform concept study to define opportunities for smart power and the potential for integrating silicon carbide, or other wide bandgap semiconductor, with silicon electronics.
- Select and optimize wide bandgap materials and processes for smart power circuits.
- Develop integration techniques for silicon carbide, or other wide bandgap semiconductor, onto silicon and/or silicon onto silicon carbide.
- Develop low on-resistance, fast switching silicon carbide power devices with hybrid control electronics.

	FY 2006	FY 2007	FY 2008	FY 2009
Submillimeter Wave Imaging FPA Technology (SWIFT)	6.850	8.168	5.260	0.000

(U) The Submillimeter Wave Imaging FPA (Focal Plane Array) Technology (SWIFT) program will develop revolutionary component and integration technologies to enable exploitation of this spectral region. A specific objective will be the development of a new class of sensors capable of low-power, video-rate, background and diffraction limited submillimeter imaging.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

(U) Program Plans:
- Develop compact, efficient, and high-power THz sources using new electronic and frequency conversion approaches.
- Develop sensitive and large format receiver arrays, advanced integration, and backend signal processing techniques.
- Develop and demonstrate a submillimeter focal plane imager.

	FY 2006	FY 2007	FY 2008	FY 2009
Technology Efficient, Agile Mixed Signal Microsystem (TEAM)	10.920	8.500	0.000	0.000

(U) Technology for Efficient, Agile Mixed Signal Microsystems (TEAM) will enable fabrication of high performance mixed signal systems-on-chip that will be the core of the embedded electronics in new platforms that are constrained by size and on-board power.

(U) Program Plans:
- Develop and demonstrate nanoscale silicon-based structures and associated fabrication processes to achieve high-speed analog/RF functions.
- Optimize device and process parameters for high speed mixed signal circuits.
- Produce test devices for analog/RF parameter extraction.
- Demonstrate Complementary Metal Oxide Semiconductor (CMOS) compatible fabrication processes that can yield integration levels greater than 10,000 nanoscale devices.
- Initiate highly parallel densely interconnected architectures with micron-sized vias penetrating stacks of detectors, analog, mixed signal and digital circuits.
- Demonstrate operation of high performance mixed signal circuits based on nanoscale devices.
- Demonstrate low noise interface and high isolation (up to 100 db) between high performance analog circuits and associated digital signal processing.
- Fabricate mixed signal systems on chip with nanoscale transistors.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

	FY 2006	FY 2007	FY 2008	FY 2009
Technology for Frequency Agile Digitally Synthesized Transmitters (TFAST)	10.000	10.120	0.000	0.000

(U) The TFAST program (Ultra High Speed Circuit Technology) will develop super-scaled Indium Phosphide (InP) Heterojunction Bipolar Transistor (HBT) technology compatible with a ten-fold increase in transistor integration for complex mixed signal circuits. Phase I established the core transistor and circuit technology to enable the demonstration of critical small scale circuit building blocks suitable for complex mixed signal circuits operating at speeds three times that currently achievable and ten times lower power. Phase II is extending the technology to the demonstration of complex (more than 20,000 transistors) mixed signal circuits with an emphasis on direct digital synthesizers for frequency agile transmitters.

(U) Program Plans:

- Develop material and process technology for super-scaled InP double heterostructure bipolar transistors (DHBTs). Technical approaches will leverage the process technology used in the silicon, and silicon germanium, industry to produce a planar, highly scalable InP HBT.
- Extend the core DHBT and interconnect technology with the implementation of complex mixed signal circuits.
- Develop super-scaled InP HBT processing technology for 0.25 micron and below.
- Develop high current, planar, InP HBTs compatible with high levels of integration.
- Develop greater than 100 GHz mixed signal circuit building blocks.
- Demonstrate record performance InP HBTs in a planar process for complex mixed signal circuits.
- Demonstrate a critical mixed signal building block circuit operating at more than 100 GHz.
- Develop circuit designs for direct digital frequency synthesizers (DDS) operating with clock speed up to 30 GHz.
- Define circuit designs and layouts for mm-wave DDS and related complex mixed signal circuits.
- Develop full circuit capability using super-scaled InP HBTs in complex (more than 20,000 transistor) circuits.
- Establish device models and critical design rules.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

	FY 2006	FY 2007	FY 2008	FY 2009
Feedback-Linearized Microwave Amplifiers	0.000	5.580	4.970	5.840

(U) Modern military platforms are requiring increased dynamic range receivers for their onboard communications, in both radar and electronic warfare antenna systems. The goal of this program is to develop RF amplifiers with revolutionary increased dynamic range receivers through the use of linear negative feedback. This program will develop the core technologies and components that may be used as building blocks and/or modules in future system applications. This program will leverage technologies from the TFAST program.

(U) Program Plans:
- Ensure stability of closed-looped amplifier while not increasing internal latencies from transistors and layout parasites.
- Address design challenges related to negative feedback.
- Investigate avoidance of circuit oscillation.

	FY 2006	FY 2007	FY 2008	FY 2009
Terahertz Imaging Focal-Plane Technology (TIFT)	9.326	13.000	7.000	0.000

(U) The TIFT program will demonstrate large, multi-element (> 40K pixels) detector receiver focal plane arrays that respond to radiation in the THz band (> 0.557 THz). The sensor system will be able to operate effectively at a standoff range (> 25m) with a high spatial resolution (< 2 cm) limited only by beam diffraction. The imaging receiver will produce a two-dimensional (2D) image in which each pixel records the relative intensity of the THz radiation received on the focal plane within the appropriate section of the field of view of the scene being sensed. The program will achieve intensity sensitivities as close as possible to the thermal background limit at room temperature. The minimal acceptable acquisition time is video-rate (30 Hz). The receiver may be either passive or active (including THz time domain methods). The size, weight, and electrical power requirements will be consistent with portability.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

(U) Program Plans:
- Demonstrate revolutionary component and integration technologies necessary for the development of a diffraction-limited, video-rate THz (at least 0.557 x 10^{12}Hz) frequency imager.
- Demonstrate a compact THz source achieving at least 10 mW of average power and 1% wall plug efficiency, as required for active illumination and/or for local oscillators in heterodyne or homodyne detection schemes.
- Demonstrate a THz receiver capable of achieving a noise equivalent power of less than 1 pW/Hz $^{1/2}$ as measured with an integrated acquisition time of no more than 30 milliseconds and a pre-detection bandwidth of no more than 50 GHz, as required in order to achieve a system-level noise equivalent delta temperature of 1K or better.

	FY 2006	FY 2007	FY 2008	FY 2009
Trusted, Uncompromised Semiconductor Technology (TrUST)	0.000	10.000	10.000	14.000

(U) The TrUST program will explore techniques to insure Integrated Circuits (IC's) of interest to the DoD can be certified as trustworthy after fabrication. These efforts will compliment other maskless lithography and verifiable design programs. The first thrust will develop new tools and techniques for rapidly analyzing fabricated circuits and comparing the circuit topology to that of the design produced at the trusted design source. The second thrust will exploit emerging research in 3D stacked and monolithic circuits to distribute, or segment, a complex IC into smaller sub-circuits. In this way, the sub-circuits can be fabricated separately, making it more difficult to compromise the complete circuit and making it easier to characterize each circuit for trustworthiness. This approach will also leverage the performance advances projected for 3D architectures. The final thrust will explore novel ways to add "hardware jacket" to complete IC's that will service to monitor the circuits' performance and raise a flag if unspecified operations are encountered.

(U) Program Plans:
- Develop new tools and techniques for rapidly analyzing fabricated circuits and comparing the circuit topology to that of the design produced at the trusted design source.
- Exploit emerging research in 3D stacked and monolithic circuits to distribute, or segment, a complex Integrated Circuit (IC) into smaller sub-circuits.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

- Explore novel ways to add "hardware jacket" to complete ICs that will service to monitor the circuits' performance and raise a flag if unspecified operations are encountered.
- Develop distributed circuit architectures by building trusted circuits through 3D segmented designs.
- Explore Integrated Circuit monitoring for deployed performance verification.

	FY 2006	FY 2007	FY 2008	FY 2009
Co-integration of Carbon-Based rf Electronics with Silicon Technology (CrEST)	0.000	0.000	4.000	5.000

(U) The CrEST program seeks to develop Metal Oxide Silicon Field Effect Transistors (MOSFETs) based on the planar carbon monolayer (graphene) system. Such a system has most of the desirable properties of carbon nanotubes, but found in a planar geometry, which is much more compatible with standard Complementary Metal-Oxide Semiconductor (CMOS) processing. The 10X mobility enhancement of graphene with respect to silicon will be exploited for high performance (high current drive) and low power electronics applications. The excellent mobility is achieved in a monolayer system which is ideal from the electrostatic (i.e., gate control) point of view enabling efficient scaling to very small device geometries. Graphene FET devices are envisioned to be an enhancement, not replacement for silicon CMOS, for critical radio frequency or mixed signal circuit elements. Thus the demonstrated integration of graphene devices into standard silicon CMOS processing is a key task of this program.

(U) Program Plans:

- Demonstrate hybrid graphene-silicon CMOS circuits for high performance and low power applications.

	FY 2006	FY 2007	FY 2008	FY 2009
Compound Semiconductor Materials On Silicon (COSMOS)	0.000	0.000	5.000	10.000

(U) The objective of the Compound Semiconductor Materials On Silicon (COSMOS) program will be to develop new methods to tightly integrate compound semiconductor technologies within silicon CMOS circuits in order to achieve such unprecedented circuit performance levels.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

Currently, heterogeneous integration of compound semiconductors with silicon is typically achieved through the use of multi-chip modules and similar assemblies. While adequate for relatively low performance applications (e.g., power amplifiers for cellular telephone handsets), the integration complexity that can be achieved in this manner is extremely limited. At the other end of the spectrum, epitaxial methods to grow III-V materials onto silicon substrates have generally proven unsatisfactory due to high defect densities, cost, and inflexibility in supporting multiple technologies. Instead, COSMOS will focus on an intermediate approach, which is likely to be the most successful strategy in terms of performance, size and cost. This will involve sub-circuit integration in which III-V materials devices are placed onto a processed CMOS wafer.

(U) Program Plans:

- Demonstrate ultralow power dissipation circuits.
- Develop methods for sub-circuit integration onto fully processed CMOS wafers.
- Evaluate alignment and bonding methods to achieve mechanical integrity of dissimilar materials, post-processing compatibility with CMOS, and the achievement of high fabrication yields.This program will greatly extend the capabilities of wide bandgap devices for use in power amplifiers (PAs) at frequencies at least as high as X-band and to make this technology useful at very high frequencies (W-band). PAPEETE will leverage advances in materials and device topologies to demonstrate large (>1 mm) devices operating in this new regime. Such high density devices will enable PAs with higher output power, fewer power combining stages, and greater efficiency than previously possible. This program will develop new means to decrease the number of optical phonons in the critical gate region of RF PA devices. Such phonon engineering should improve high power performance.

	FY 2006	FY 2007	FY 2008	FY 2009
Steep-subthreshold-slope Transistors for Electronics with Extremely-low Power	0.000	0.000	5.000	7.000

(U) The Steep-subthreshold-slope Transistors for Electronics with Extremely-low Power (STEEP) program seeks to develop field emission (tunneling) based Metal Oxide Silicon Field Effect Transistors (MOSFETs). Such devices would enable lowering supply voltages by 5X which would result in an active power savings of 25X and a standby power saving of at least 5X. Prototype circuits will be developed showing such power savings with little to no impact on performance (current drive). Such field emission devices will be integrated into standard CMOS based processing methods and offer significant CMOS power reduction with no performance penalty.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

(U) Program Plans:
- Develop novel MOSFET switch with significantly steeper sub-threshold slope.
- Develop CMOS process integration.
- Optimize drive current in presence of tunneling barrier.
- Demonstrate ultra-low power, high performance prototype circuits.

	FY 2006	FY 2007	FY 2008	FY 2009
Semiconductor-Tuned HTS Filters for Ultra-Sensitive RF Receivers (SURF)	0.000	0.000	3.343	7.900

(U) The operation of frequency-hopping radios greatly interferes with co-located ultra-sensitive receivers. The situation will get worse as the "hoppers" proliferate, even interfering within the receive channels of one another. A general solution would be to use "brick-wall" front-end filters for the receivers, re-tuning at the rate of the hoppers. High-temperature superconducting (HTS) filters have been used very successfully for negating strong transmissions at nearby frequencies, and are unique in their ability to totally reject out-of-band signals without attenuation of signals in the pass-band. However, they have been used only for rejection of fixed-frequency interference. This program would increase the turning speed of HTS filters, from about a second with present mechanical methods, to microsecond speeds required for systems such as the Joint Tactical Information Distribution System (JTIDS). The technology for such a million-fold improvement will rely upon semiconductor tuning, properly mated with the superconducting filter materials. In addition to interference-rejection at microsecond speeds, these filters will make it possible to perform wide spectral searches with unprecedented frequency resolution, enabling detection of very weak emissions (signatures) characteristic of threat systems.

(U) Program Plans:
- Develop the technology of semiconductor filters, employing either varactor tuning or switched capacitor banks, in integrated-circuit format.
- Demonstrate semi-continuous tuning over a 10 percent bandwidth, with stepwise (switching) semiconductor retuning at microsecond speeds.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

– Demonstrate continuous tuning of HTS notch filters at microsecond speeds, adequately negating interference from co-located transmitters over the receive frequency band.

	FY 2006	FY 2007	FY 2008	FY 2009
Adaptive Focal Plane Arrays (AFPA)	5.170	8.039	5.870	5.275

(U) The goal of this program is to demonstrate high-performance focal plane arrays that are widely tunable across the entire infrared (IR) spectrum (including the short, middle and long-wave infrared bands), thus enabling "hyperspectral imaging on a chip." The Adaptive Focal Plane Array (AFPA) program will also allow for broadband Forward Looking Infrared (FLIR) imaging with high spatial resolution. These AFPAs will be electrically tunable on a pixel-by-pixel basis, thus enabling the real-time reconfiguration of the array to maximize either spectral coverage or spatial resolution. The AFPAs will not simply be multi-functional, but rather will be adaptable by means of electronic control at each pixel. Thus, the AFPAs will serve as an intelligent front-end to an optoelectronic microsystem. The AFPA program outcome will be a large format focal plane array that provides the best of both FLIR and Hyper-Spectral Imaging (HSI).

(U) Program Plans:
- Develop component technology (tunable IR photodetectors).
- Integrate detector array.
- Demonstrate pixel-by-pixel electrical tunability in IR.
- Demonstrate AFPA prototype field using a large format array.

	FY 2006	FY 2007	FY 2008	FY 2009
Advanced Precision Optical Oscillator (APROPOS)	6.614	6.020	4.200	0.000

(U) The APROPOS program will leverage advances in materials and lasers to develop new precision microwave-stable local oscillators with extremely low phase noise (up to 50 dB better than the current state of the art) at small offsets from microwave carrier frequencies. This capability

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

will enhance performance of radars in the detection of slow moving targets; electronic warfare systems in the identification of specific emitters and communication systems in weak signal detection and clutter suppression all at increased standoff range.

(U) Program Plans:
- Improve phase noise power spectral density by 25 dB and prove the utility of multi-line laser cavities and opto-electronic oscillators.
- Identify and characterize environmental susceptibilities and define path to 50 dB improvement over state-of-the-art.
- Demonstrate 50 dB improvements in lab setting.
- Develop miniaturization approach and packing concept to mitigate environmental susceptibilities.
- Miniaturize devices in ruggedized packages.
- Demonstrate performance in tactical environments by inserting laser cavities or oscillators in system testbeds.

	FY 2006	FY 2007	FY 2008	FY 2009
Analog Optical Signal Processing (AOSP)	3.989	0.000	0.000	0.000

(U) Analog Optical Signal Processing (AOSP) significantly enhanced the performance and enabled new capabilities and architectures for tactical and strategic RF systems. The program expanded the dynamic range-bandwidth and time-bandwidth limits by a factor of 1,000 through the introduction of analog optical signal processing components into the system front ends.

(U) Program Plans:
- Designed, fabricated and tested individual photonic components capable of meeting RF signal processing requirements.
- Determined the most promising approaches for development of integrated, chip-scale components using new materials and processing technologies.
- Down-selected the most promising approaches and completed prototype module assembly.
- Constructed testbeds capable of fully characterizing the photonic-based RF signal processing components.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

	FY 2006	FY 2007	FY 2008	FY 2009
Bio-Electronics and Photonics	0.000	4.000	5.000	5.000

(U) The Bio-Electronics and Photonics program will demonstrate new capabilities in protein- and DNA-based optical and electronic media that will address the challenge of high density storage without loss of rapid access time.

(U) Program Plans:

- Develop new synthetic or engineered natural chromophores that possess both sufficient chromophore density and optical cross-section.
- Use DNA as a low loss cladding layer for electro-optic (EO) devices, i.e., waveguides.
- Demonstrate sub-wavelength addressing techniques.
- Demonstrate high density, rapid access logic gates and memories.

	FY 2006	FY 2007	FY 2008	FY 2009
Chip-to-Chip Optical Interconnects	4.709	1.000	0.000	0.000

(U) Continuing advances in integrated circuits technology are expected to push the clock rates of Complimentary Metal Oxide Semiconductor (CMOS) chips into 10GHz range over the next five-to-seven years. At the same time, copper-based technologies for implementing large number of high speed channels for routing these signals on a printed circuit board and back planes are expected to run into fundamental difficulties. This performance gap in the on-chip and between-chip interconnection technology will create data throughput bottlenecks affecting military-critical sensor signal processing systems. To address this pressing issue, this program will develop optical technology for implementing chip-to chip interconnects at the board and back plane level.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

(U) Program Plans:
- Develop high-linear density, low loss optical data transport channels that can be routed to ~1 meter distance in a geometric form factor compatible with a printed circuit board.
- Demonstrate high speed (faster then 10 GBps), low power (less then 50 mW) optical transmitters/receivers.
- Integrate optical transmitters/receivers and optical data paths with electronic packaging and manufacturing approaches.

	FY 2006	FY 2007	FY 2008	FY 2009
Photonic Analog Signal Processing Engines with Reconfigurability (PhASER)	0.000	0.000	5.000	8.000

(U) The goal of the Photonic Analog Signal Processing Engines with Reconfigurability (PhASER) program is the creation of new Photonic Integrated Circuit (PIC) elements, and associated programmable filter array concepts that will enable high-throughput, low-power signal processors. The focus is on the development of novel "Unit Cells," which may be used as building blocks to synthesize arbitrarily complex filters within a PIC platform for ultra-high bandwidth signal processing applications.

(U) Program Plans:
- Define and design a novel analog photonic "Unit Cell," which is nominally comprised of a sub-array of waveguide-connected programmable active elements. The Unit Cell should be externally linkable with integrated waveguides, which will allow it to function as a building block in programmable PIC arrays for generalized high-order finite impulse response/infinite impulse response (FIR/IIR) filters.
- Demonstrate an experimental Unit Cell concept.
- Determine how the Unit Cell, when arrayed within a high-density PIC, will perform. Develop a filter synthesis tool to demonstrate how Unit Cells will enable generalized high-order filters, and how they will be programmed and tested at the chip-level to ensure high yield.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

	FY 2006	FY 2007	FY 2008	FY 2009
Linear Photonic RF Front End Technology (PHOR-FRONT)	0.000	4.594	5.385	5.000

(U) The goal of this program is to develop photonic transmitter modules that can adapt their frequency response and dynamic range characteristics to mate with the full spectrum of narrow-band and broadband microwave transmission applications covering the 2 MHz – 20 GHz range. These field programmable, real-time adaptive photonic interface modules will find application in high dynamic range communications, radar and Electronic Warfare (EW) antenna applications.

(U) Program Plans:

- Develop photonic transmitter modules to allow tunable frequency and impedance matching to arbitrary antenna structures with adaptive pre-distortion, feedback and feed-forward linearization schemes.
- Transition into airborne, space and maritime platforms where wideband communications, radar and EW apertures with size, weight and power advantages are needed.

	FY 2006	FY 2007	FY 2008	FY 2009
Optical Arbitrary Waveform Generation (OAWG)	6.735	9.482	7.414	4.000

(U) The ultimate vision for the Optical Arbitrary Waveform Generator (OAWG) program is to demonstrate a compact, robust, practical, stable octave-spanning optical oscillator, integrated with an encoder/decoder capable of addressing individual frequency components with an update rate equal to the mode-locked repetition rate. This would provide an unprecedented level of performance for optical systems, and enable numerous high level applications including sub-diffraction-limited imaging and ultra-wideband optical communications.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

(U) Program Plans:
- Demonstrate technology for producing (and detecting) arbitrary coherent optical waveforms with > with positive linear chirp of 1000 GHz with fidelity of <5% least-squared deviation from mathematical ideal waveform, accounting for interference from adjacent waveforms.
- Demonstrate production of single-cycle, 3 GHz square wave (pulse train duration of 0.67 ns) with fidelity of <1% least-squared deviation from mathematical ideal waveform.

	FY 2006	FY 2007	FY 2008	FY 2009
Technology for Agile Coherent Optical Transmission & Signal Processing (TACOTA)	4.995	6.705	5.700	0.000

(U) The goal of TACOTA (formerly called Optoelectronics for Coherent Optical Transmission and Signal Processing) is to develop optoelectronic component technologies that enable increased physical layer security in optical transmission systems through the synergistic use of coherent optical technologies and high-speed electronics. Secure, high-capacity free-space communications is essential for the transformational communications architecture to be realized. Both digital and analog transmission will be considered.

(U) Program Plans:
- Develop compact stable lasers, local oscillators and frequency combs (<10 Hz linewidths with <1 kHz long-term accuracy), high-speed quadrature optical modulators (>6 bit/s/Hz spectral efficiency with 100 GHz signaling rates), and digital homodyne receivers.
- Transition into airborne, space and maritime platforms where secure, high-capacity military optical networks for targeting and imaging are coveted.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

	FY 2006	FY 2007	FY 2008	FY 2009
Solid State Imager/Extended Range Materials/Long WL High Grain Optical Sensors	2.000	3.000	0.000	0.000

(U) Imaging in the near-to-mid Wave Length (WL) spectral region provides the capability to penetrate atmospheric obscurants, where conventional sensors cease to generate data or produce severely degraded information. New materials and concepts for solid state imaging are essential to take advantage of this novel imaging regime, providing the capability to see where others cannot. This development includes new material concepts, such as quantum dots and superlattice structures, which offer the ability to precisely tailor the spectral band, and potentially operate at or near room temperature. In addition, new solid state sensor concepts will be developed to spatially and temporally co-register each pixel in the image to implement novel on-chip processing for noise cancellation and clutter rejection in severely degraded environments.

(U) Program Plans:
- Develop new material concepts.
- Develop new solid state sensors concepts.

	FY 2006	FY 2007	FY 2008	FY 2009
Ultrabeam	1.344	1.000	0.000	0.000

(U) The Ultrabeam program involves conversion of femtosecond duration ultraviolet laser light pulses to x-rays and the study of intense x-ray pulse propagation in various media.

(U) Program Plans:
- Validate the scientific feasibility of the conversion and propagation processes.
- Demonstrate a working laboratory model involving higher beam energies and shorter pulse durations.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

	FY 2006	FY 2007	FY 2008	FY 2009
Ultra-WideBand A/D Conversion (UWB-ADC)	0.000	0.000	5.235	7.445

(U) The objective of UWB-ADC is to develop revolutionary technologies to enable Analog to Digital Converters (ADCs) with high-resolution and large instantaneous bandwidth while maintaining power consumption that is commensurate with user community requirements. It is expected that such ADCs would have a dramatic impact on SIGINT capabilities such as direct down conversion of UHF through X-band RF signals. Furthermore, ADCs enabled by UWB-ADC alleviate the current ADC bottleneck in high capacity digital RF communications links by enabling more spectrally efficient wideband waveforms. This program aims to develop a bandwidth-compressing photonic front end that provides a force multiplier for any available back-end electronic ADCs.

(U) Program Plans:
- Emphasize photonic time-stretch analog-to-digital converter (TS-ADC) technology.
- Develop multi-channel time stretching technologies for continuous time signals.
- Develop components mandated by system-level ADC specifications.

	FY 2006	FY 2007	FY 2008	FY 2009
Novel Technologies for Optoelectronics Materials Manufacturing (NTOMM)	0.000	0.000	3.750	6.000

(U) The goal of the Novel Technologies for Optoelectronics Materials Manufacturing (NTOMM) program is to develop and demonstrate new technologies for Group II-VI (e.g., Cadmium Selenide (CdSe)) and III-V (e.g., Gallium Nitride (GaN) materials and device manufacturing, enabling imaging and emissive device fabrication at 1% to 10% current costs. This advance will dramatically expand the application space of such devices, enabling lower cost per large area IR imaging systems, non-planar devices and systems, and thin film and flexible devices and systems. This program will demonstrate IR detectors and imagers, Light Emitting Diodes, and solid state lasers fabricated via new methods, and include a rapid demonstration of at least 5x reduction in yielded device cost. The NTOMM program will leverage recent and ongoing developments in

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

nano-material synthesis and assembly, which have demonstrated the potential for over 50% precursor stream usage in the fabrication of II-VI and III-V materials.

(U) Program Plans:
- Develop synthesis methods that improve quality and monodispersity (characterized by particles of uniform size in a dispersed space) of InN and InGaN nanocrystals.
- Develop cost effective synthesis methods for Group II-VI and III-V materials.
- Utilize controlled arrays of InGaN to form high efficiency Light Emitting Diode (LED) structures and imaging sensors in IR.
- Assemble layer-by-layer heterostructures (characterized by dissimilar materials with non-equal band gaps) from ordered planar arrays of nanocrystals.
- Develop and demonstrate techniques for layer doping of heterostructure materials.

	FY 2006	FY 2007	FY 2008	FY 2009
Optical Antenna Based on Nanowires	0.000	0.000	2.000	4.000

(U) In optics, nanotechnology research will develop the ability to create structures of the same scale as incident light wavelengths. These structures can interact with and affect the incident light. This program will create nano-meter scale structures, which will act as optical antenna arrays that can respond coherently to electromagnetic fields at optical wavelengths. Each array element would be a nanostructure, such as a nanotube or nanowire, and provide a way to measure directly the field magnitude and phase in both space and time. A system based on this technology would potentially be smaller, lighter in weight, and able to move from the sub-optimal method of intensity-only measurements into the information-rich domain of complex imaging.

(U) Program Plans:
- Develop and demonstrate small element count two-dimensional array, characterize performance and scaling relationships.
- Demonstrate and characterize ability to measure the magnitude and phase of the incident light.
- Demonstrate image formation capability.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

– Design, develop, and test a prototype system.

	FY 2006	FY 2007	FY 2008	FY 2009
3-D Microelectromagnetic RF Systems (3-D MERFS)	5.804	3.960	1.750	1.000

(U) The 3-D Microelectromagnetic RF systems (3-D MERFS) program will develop complete millimeter wave (MMW) active arrays on a single or a very small number of wafers. The program will exploit new technologies being developed commercially that allow Gallium Arsenide (GaAs) active components to be placed on Silicon wafers, and advances in Indium Phosphide and Silicon Germanium that may allow an entire MMW Electronically Scanned Array (ESA) to become very highly integrated on a sandwich of wafers. At lower frequencies, the large spacing between radiating elements precludes the efficient use of the wafer real estate for fabricating the entire ESA, but at Ka and W- bands, the element spacing is small enough to allow an ESA to be made with active transmit/receive chips and control circuits on one layer, radiators on another, and a feed system on a third. This could potentially make them very cheap, compact, lightweight and reliable. This would enable the development of new MMW ESAs of a six inch diameter or less for seekers, communication arrays for point-to-point communications, sensors for smart munitions, robotics and small remotely piloted vehicles. This program will build upon technology developed under the Vertically Interconnected Sensor Array program.

(U) Program Plans:
- Survey the emerging commercial MMW technology base and identify the best candidate processes for the MMW ESA application.
- Develop the optimal ESA architectures for wafer fabrication.
- Determine requirements for MMW ESAs that match the expected performance.
- Design, build, and test candidate ESA designs.
- Design, build, and test full ESA seeker or other system using the wafer fabrication technology.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

	FY 2006	FY 2007	FY 2008	FY 2009
Chip Scale Atomic Clock	4.023	5.000	8.000	8.000

(U) The Chip Scale Atomic Clock will demonstrate a low-power chip scale atomic-resonance-based time-reference unit with stability better than one part per billion in one second. Application examples of this program will include the time reference unit used for GPS signal locking.

(U) Program Plans:
- Demonstrate feasibility and theoretical limits of miniaturization of cesium clock.
- Demonstrate subcomponent fabrication including atomic chamber, excitation and detection function.
- Demonstrate design and fabrication innovation for atomic-confinement cell and for GHz resonators suitable for phase locking or direct coupling with atomic confinement cell.

	FY 2006	FY 2007	FY 2008	FY 2009
Radioisotope Micropower Sources (RIMS)	2.056	2.289	3.021	0.997

(U) This effort will seek to develop the technologies and system concepts required for safely producing electrical power from radioisotope materials for portable and mobile applications, using materials that can provide passive power generation. There will also be research in compact radioisotope battery approaches that harness MEMS technology to safely and efficiently convert radioisotope energy to either electrical or mechanical power while avoiding lifetime-limiting damage to the power converter caused by highly energetic particles (e.g., such as often seen in previous semiconductor approaches to energy conversion). The goal is to provide electrical power to macro-scale systems such as munitions, unattended sensors, and weapon systems, RF ID tags, and other applications requiring relatively low (up to tens of milliwatts) average power. This program formerly funded the Micro Isotope Micro-Power Sources (MIPS) program, which has been broken out as a separate program and separately described in this exhibit.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

(U) Program Plans:
- Developed and demonstrated core technologies of radioisotopes and the manufacturing of alpha and beta capture mechanisms.
- Develop large-scale radioisotope generation cell based on alpha and beta particle capture.
- Demonstrate advances in power output at high conversion factors, material stability, and particle capture in a small form factor with high conversion efficiencies, while operating within safety considerations and limitations.
- Demonstrate reasonable longevity for the chosen radioisotope-to-electrical or radioisotope-to-mechanical power conversion technique.
- Demonstrate actual, long-lasting power generation by the chosen radioisotope-to-electrical or radioisotope-to-mechanical conversion method.

	FY 2006	FY 2007	FY 2008	FY 2009
Micro Isotope Micro-Power Sources (MIPS)	1.650	2.375	4.000	5.000

(U) The goal of the MIPS program is to demonstrate safe, affordable micro isotope power sources able to outperform conventional batteries in terms of energy and/or power density, and provide long lasting milliwatt (mW)-level power for an array of critical military applications, such as unattended sensors, perimeter defense, detection of weapons of mass destruction (WMD), and environmental protection.

(U) Program Plans:
- Evaluate the applicability of known and potential sources to critical applications faced by the department. Analyze the feasibility and cost of manufacturing for these sources and compare against benefit derived for each application.
- Investigate a range of approaches to achieving compact, milliwatt-level power sources including alphavoltaic, betavoltaic, and thermoelectric strategies.
- Demonstrate power conversion devices able to meet relevant size, power, and safety constraints for potential applications.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

	FY 2006	FY 2007	FY 2008	FY 2009
Surface Enhanced Raman Scattering (SERS) - Science and Technology	0.000	0.000	5.000	8.000

(U) Surface Enhanced Raman Scattering (SERS) – Science and Technology program focuses on the fundamental technical challenges facing potential sensor performance with respect to their sensitivity, selectivity, enhancement factors and development. SERS nanoparticles have considerable potential for both chemical and biochemical sensing applications due to: (1) their potential large spectral enhancement factors, (2) the nature of spectral fingerprints that can be expected to yield low false alarm rates, and (3) the capability for detecting targeted molecules at useful standoff ranges. This program seeks to identify and overcome the key scientific and technical challenges necessary for replacing existing sensors of chemical and biological warfare (CBW) agents with SERS-based sensing approaches.

(U) Program Plans:

- Develop understanding of nanoparticle shape and its effect on SERS enhancements; examine high quality resonators for SERS applications.
- Develop methods to engineer nanoparticles with 1 nanometer feature sizes (separation) on a macroscale.

	FY 2006	FY 2007	FY 2008	FY 2009
Design Tools for 3-Dimensional Electronic Circuit Integration	13.634	10.272	7.474	0.000

(U) This program will develop a new generation of Computer Aided Design (CAD) tools to enable the design of integrated three-dimensional electronic circuits. The program will focus on methodologies to analyze and assess coupled electrical and thermal performance of electronic circuits and tools for the coupled optimization of parameters such as integration density, cross talk, interconnect latency and thermal management. The goals of this initiative are to develop a robust 3-D circuit technology through the development of advanced process capabilities and the design tools needed to fully exploit a true 3-D technology for producing high performance circuits. The deliverables from this program will have a significant impact on the design of mixed signal (digital/analog/RF) systems and Systems-on-a-Chip for high performance sensing, communications, and processing systems for future military requirements.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

(U) Program Plans:
- Apply 3D design tools to test structure.
- Fabricate and test structures.
- Verify models against data.

	FY 2006	FY 2007	FY 2008	FY 2009
Multiple Optical Non-Redundant Aperture Generalized Sensors (MONTAGE)	4.070	3.248	0.000	0.000

(U) The MONTAGE program will implement a revolutionary change in the design principles for imaging sensor systems, enabling radical transformation of the form, fit, and function of these systems for a wide variety of high-value DoD applications. Significant improvements in the performance, affordability, and deployability of imaging sensor systems will be obtained through rational co-design and joint optimization of the imaging optics, the photo sensor array and the post-processing algorithms. By reaching well beyond conventional designs, MONTAGE sensors will realize optimal distribution of information handling functions between analog optics and digital post-detection processing.

(U) Specific demonstrations include reduction of the depth/thickness of an imaging sensor by an order of magnitude without compromising its light gathering ability or resolution. This dramatic reduction in thickness will then allow the imaging sensors to be deployed conformally around a curved surface of a platform (e.g., UAV, tank, or helmet). Furthermore, the flexibility generated by the incorporation of post-processing in the image formation will allow variable resolution image formation, which in turn reduces the data load for subsequent image exploitation and communication systems. Advanced post-processing algorithms will support video operation at frame rates in excess of 10 frames per second using standard computing platforms.

(U) Program Plans:
- Develop novel optical designs allowing depth reduction by 10X.
- Concurrent with optics design, develop sensor array design and post-processing algorithms to realize signal-to-noise ratio and resolution of comparable optical aperture.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

- Demonstrate ability to allocate highest spatial resolution to specified regions of interest in the image while maintaining medium resolution elsewhere.
- Develop architectures for surpassing detector size-limited resolution and potentially exceed optically limited resolution.
- Demonstrate operation of a thin imaging system deployed on a curved surface.
- Demonstrate real time performance of thin imaging systems in representative DoD applications with performance evaluated using application-specific metrics for image quality, sensor cost, power consumption, mechanical properties.

	FY 2006	FY 2007	FY 2008	FY 2009
Polymorphous Computing Architecture (PCA)	11.392	5.802	8.000	14.000

(U) The Polymorphous Computing Architectures (PCA) program is developing a revolutionary approach to the implementation of embedded computing systems to support reactive multi-mission, multi-sensor, and in-flight retargetable missions. This revolutionary approach will reduce payload adaptation, optimization and verification processes from years to minutes. The program breaks the current development approach of hardware first and software last by moving beyond conventional silicon to flexible polymorphous computing systems. The key efforts of this revolutionary step forward in embedded computing systems are: (1) define critical reactive computing requirements and critical micro-architectural features; (2) explore, develop and prototype reactive polymorphous computing concepts; (3) explore, develop and prototype multi-dimensional verification and validation techniques for dynamic reactive missions; (4) provide early experimental testbeds and prototype polymorphous computing systems; and (5) extend PCA to enable early commercial product development and transition to the DoD and intelligence communities. The result will be a significant breakthrough in DoD warfighter capability.

(U) Two promising PCA architectures, eXtended Tera-op Reliable Intelligently Adaptive Processing System (TRIPS) and eXtended MOrphable Networked microARCHitecture (MONARCH), will bridge the gap between the prototypes developed in the PCA program and provide transition-ready solutions that can be adopted by DoD and intelligence agencies. This effort includes performing product-level development of processor chips, multi-modules and software development environments planned for future deployment by DoD and intelligence end users.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

(U) This research effort will also extend the polymorphic research into developing a silicon compiler targeted at "maskless lithography." Recent work in "maskless lithography" shows promise for avoiding the time and costs associated with the complex masks currently required for digital chip development. In addition, this technique would allow 'system on a wafer' development to support low volume systems while providing low cost production and quick turnaround.

(U) Additionally, as more and more chip fabrication is outsourced and the U.S. becomes more susceptible to faults and malicious hardware components, the need for autonomously adaptive mechanisms has become apparent as another extension of the PCA program. The self monitoring hardware in conjunction with co-developed software will incorporate cognitive techniques to determine the state and health of the processor, and based on the evaluation, will reconfigure, correct or shut down the processor to minimize the impact of a fault or malicious hardware. This self-aware trusted computing technology will enable the delivery of a more robust, self correcting trustable computing system.

(U) The resulting PCA technology will mark a new generation of on-board, embedded computing processing capabilities that will be mission and technology agnostic yet highly optimizable for each new mission scenario. This processing capability will provide tactical and strategic mission tempo opportunities as well as technical upgradeability over the life of the computing system. Based on an average of four major upgrades over a 30-year period, significant savings of up to 45 percent in development and deployment costs may be achieved over the life of a typical DoD embedded computing system.

(U) Program Plans:

- Fabricated and delivered the xMONARCH chip.
- Prototype and evaluate the TRIPS chip for implementing novel TRIPS Explicit Data Graph Execution architecture and the TRIPS compiler for implementing backend optimizations.
- Model, simulate and characterize complete candidate polymorphic computing systems including hardware elements, morphware, run-time systems and tools.
- Perform early small scale proof-of-concept testing, integration and evaluation of early polymorphic computing architecture prototypes.
- Demonstrate and quantify the potential of full up polymorphic computing architecture systems for the DoD and their complementary commercial viability.
- Select, develop, and perform a DoD risk reduction effort for a multi-mission application.
- Set the stage for technology transition to commercial and defense contractor communities in support of DoD applications.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

- Perform early commercial product development and transition to the DoD and intelligence on-board embedded processing communities.
- Create a unique development environment chain - the silicon compiler - from high level application representation to implementation using a breakthrough high-speed, high-yield maskless lithography fabrication approach.
- Initiate a study to identify potential new hardware architectures and candidate approaches, such as master/slave methods where the "slave" collects and condenses data.
- Explore techniques to enable computing systems to self-monitor their state, identify unexpected or unwanted system behavior, and transparently adapt in real time.

	FY 2006	FY 2007	FY 2008	FY 2009
Vertically Interconnected Sensor Arrays (VISA)	3.995	5.200	3.000	2.500

(U) The Vertically Interconnected Sensor Arrays (VISA) program will develop and demonstrate vertically interconnected, focal plane array (FPA) read-out technology capable of more than 20-bits of dynamic range, enabling significant advances in the functionality of infrared systems. The extremely high dynamic range will be accomplished by novel multilayer read-out circuits. These circuits will enable imaging at more than 20-bits of dynamic range, whereas the current state of the art is over an order of magnitude lower. Adaptive read-out circuits will be vertically connected to individual detectors in either monochromatic or stacked multicolor 2D staring arrays. The ability to bring signals directly from the detectors to the read-outs (i.e., vertical interconnection) without first going through row-column multiplexers will allow for high frame rates concurrently with high resolution images. A companion application-oriented program is funded in PE 0603739E.

(U) Program Plans:

- Develop a wafer stacking process incorporating high-density vias and design novel circuits that enable high frame rates, counter-measure hardening and adaptive signal processing functions on a concept test chip.
- Demonstrate a high dynamic range Analog/Digital VISA technology based sensor designed with advanced high performance circuit architecture implemented in stacked semiconductor process with high-density interconnections.
- Determine the best bands for improving the detection of objects in varying degrees of fog.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

	FY 2006	FY 2007	FY 2008	FY 2009
Lidar on a Chip	0.000	0.000	3.500	5.000

(U) The Lidar on a Chip program will develop a lidar system based on novel chip technologies/architectures resulting in significantly reduced (>> 10X) lidar system size, cost, and weight. Technology will be developed to allow both photonics and electronics to be fabricated on the same substrate, enabling the laser, signal processing, supporting subsystem components and the transmit and receive beam components to be implemented as chip-scale elements. This technology will enable the development of small-scale seeker systems. Reducing the size, weight and cost of a lidar system will revolutionize precision targeting systems.

(U) Program Plans:
- Develop and demonstrate fabrication technology.
- Demonstrate functional performance of array in laboratory scale devices.
- Develop and demonstrate brassboard array performance and scaling relationships.
- Design, develop, and test a prototype system.

	FY 2006	FY 2007	FY 2008	FY 2009
Structured ASIC Design (StASD)	0.000	0.000	3.500	5.500

(U) Currently Application Specific Integrated Circuits (ASIC) have a 20-30X performance advantage over general-purpose programmable processors, which is critical for high performance systems and platforms. The current ASIC design solutions are high in cost, require extensive time to design, apply to a single application, and need dedicated hardware, making them unattainable for most critical DoD systems. Also, when customizing ASICs for multiple applications, the overhead costs greatly increase in terms of performance density, clock speeds, and high power. The development of a Structured ASIC Design will provide the performance advantages of a customized ASIC but without the high overhead costs of programmable or fine-grain reprogrammable devices. The result will be highly novel, customizable ASICs that will dramatically enhance DoD applications in terms of cost, time to design, and performance.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

(U) Program Plans:
- Determine which common high performance functional elements provide the best option for high performance functionality at the appropriate level and capability of interconnects for the optimal customization.
- Characterize, identify and implement interconnects to customize devices to the application.
- Develop an ASIC implementation-based functionality layer to provide common, high-performance ASIC functional elements.

	FY 2006	FY 2007	FY 2008	FY 2009
Cognitively Augumented Design for Quantum Technology (CAD-QT)	1.120	2.000	0.000	0.000

(U) The Cognitively Augmented Design for Quantum Technology (CAD-QT) study phase program has developed learning-based optimization tools and represents a stepping stone towards an intelligent search engine capable of guiding the designer through the complex trade spaces of quantum device design.

(U) Program Plans:
- Validate CAD-QT system by employing it to design optoelectronic modulator devices performing significantly beyond the current state of the art.
- Investigate the exploitation of new fields of nanophotonics and plasmonics in which metal nanostructures convert electromagnetic radiation into charge density waves.

	FY 2006	FY 2007	FY 2008	FY 2009
Direct Analog To Target ID - Non-Linear Math for Mixed Signal Microsystems	7.401	6.302	3.089	0.000

(U) The principal goal of this program is to demonstrate a significant linearity enhancement capability based upon a digital signal processing approach, implemented in a high performance, very large scale integration (VLSI) chip that will enable wideband high-dynamic range sensor systems to be developed in a cost effective manner.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

(U) Program Plans:
- Develop broadly applicable methodologies for exploiting novel encoding strategies, closed loop adaptive equalization, integration of sensing and processing, and application-specific knowledge in order to provide revolutionary advances in information conversion.
- Explore novel architectures leveraging intelligent pre-processing based upon space, time, and mathematical transformations of analog measurements and employing cooperative integration of analog and digital processing to obtain required system level performance.
- Work with new classes of quantization devices based on novel "error correcting" representations of numbers, such as beta encoders, phase encoders, geometric invariants.

	FY 2006	FY 2007	FY 2008	FY 2009
Reliable Efficient Scalable Computing with Unreliable Elements (RESCUE)	0.000	0.000	4.000	5.000

(U) This program will develop hierarchical error correction and redundancy mechanisms right down to the gate level to compensate for device level errors and deliver reliable computing performance from Probabilistic-Complementary Metal Oxide Semiconductors (P-CMOS) devices scaling towards intrinsic statistical imperfection. These novel approaches will be adjustable to provide accuracy according to the requirements of particular applications, enabling optimization of power-performance trades at the level. Particular targets for applications will be high performance embedded signal and image processing tasks including radar image formation, video compression, and speech recognition. The RESCUE program will help sustain the advantages of Moore's law scaling for a wide variety of DoD's critical embedded signal processing and analysis applications. Significant benefits in energy reduction without loss of performance will be available almost immediately.

(U) Program Plans:
- Devise P-CMOS computational building blocks and primitives such as Finite Impulse Response (FIR) filter, Fast Fourier Transformer (FFT), on up to Synthetic Aperture Radar (SAR) processing.
- Develop systematic automation for support of non-uniform probabilistic design.
- Characterize tradeoff between application quality and savings through novel metrics such as Energy-Performance Product (EPP).
- Demonstrate defect-tolerant probabilistic adder design.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

– Perform error correction through augmented probabilistic designs, including use of Chernoff tail bounds to contain redundancy. Use duality to extend temporal (noise) variations to spatial (parameter) variations (e.g., dual threshold voltages).

	FY 2006	FY 2007	FY 2008	FY 2009
National Secure Foundry Initiative	1.200	2.000	0.000	0.000

(U) The Secure Advanced Fabrication Facility for Electronics (SAFFE) aims to support and develop nanoelectronics innovations in support of homeland security and national defense applications, with target products ranging from power electronics systems, advanced superconductors, integrated "nanochip" solutions for lithography, 3-D integration, device modeling and simulation, and metrology applications. Scaling down of semiconductor device feature sizes has led to advanced electronic components and new capabilities for signal and data processing. This program pursued research concepts for shrinking semiconductor devices to the nanoscale and explored applications to integrated microsystems.

	FY 2006	FY 2007	FY 2008	FY 2009
Semiconductor Nanoelectronics Research	0.500	0.000	0.000	0.000

(U) Scaling down of semiconductor device feature sizes has led to advanced electronic components and new capabilities for signal and data processing. This program pursued research concepts for shrinking semiconductor devices to the nanoscale and explored applications to integrated microsystems.

	FY 2006	FY 2007	FY 2008	FY 2009
Characterization, Reliability & Applications for 3-D Microdevices	0.000	2.600	0.000	0.000

(U) Develop innovative processing instrumentation for the fabrication of Three-Dimensional (3-D) Microdevices.

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E

	FY 2006	FY 2007	FY 2008	FY 2009
3D Technology for Advance Sensor Systems	0.000	2.200	0.000	0.000

(U) Explore 3D Technology innovation for application to Advance Sensor Systems.

(U) **Program Change Summary:** *(In Millions)*	**FY 2006**	**FY 2007**	**FY 2008**	**FY 2009**
Previous President's Budget	239.959	246.978	244.651	244.775
Current Budget	220.011	239.370	213.529	219.844
Total Adjustments	-19.948	-7.608	-31.122	-24.931
Congressional program reductions	-13.800	-14.408		
Congressional increases	0.000	6.800		
Reprogrammings	0.000			
SBIR/STTR transfer	-6.148			

RDT&E BUDGET ITEM JUSTIFICATION SHEET (R-2 Exhibit)	DATE February 2007
APPROPRIATION/BUDGET ACTIVITY RDT&E, Defense-wide BA2 Applied Research	R-1 ITEM NOMENCLATURE Electronics Technology PE 0602716E, R-1

(U) Change Summary Explanation:

FY 2006	The decrease reflects the SBIR/STTR transfer and the Section 8040 rescission.
FY 2007	The decrease reflects congressional cuts to the following programs: Clockless Logic, Metaphoric Computing, Advanced Digital Receiver Technology, TEAM, Terahertz Imaging Focal-Plane Technology, AFPA, Bio-Electronics and Photonics, Linear Photonic RF Front End Technology, Multiple Optical Non-Redundant Aperture Generalized, and a reduction for Section 8106 Economic Assumptions. The decreases are offset by congressional adds to: SAEF, 3-D Technology for Advanced Sensor Systems, and Innovative Processing Instrumentation for Fabrication of 3-D Microdevices.
FY 2008/2009	Decrease reflects overall funding reductions resulting from rephasing of outyear milestones.

(U) Other Program Funding Summary Cost:

- Not Applicable.